Digital-IF WCDMA Handset Transmitter IC in 0.25-μm SiGe BiCMOS

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***Abstract*—Implemented in a 0.25-μm SiGe BiCMOS process, a highly integrated low-power transmitter IC (TxIC) is developed for wideband code-division multiple-access handset applications. Based on a digital-IF heterodyne architecture, it eliminates the external IF surface acoustic wave filter by adopting a meticulous frequency plan and a special-purpose second-order-hold D/A conversion scheme. The TxIC features a low-power high-speed D/A converter designed to drive a dominantly capacitive load. For the upconversion mixer and the RF amplifier, adaptive biases are designed to minimize the quiescent power consumption and to provide current boost only when needed. The TxIC achieves $<1\%$ EVM. It consumes 180 mW (3-V supply) for the maximum output power of $+5$ dBm and reduces to 120 mW during power backoff.**

***Index Terms*—Digital-IF, digital-to-analog converter (DAC), heterodyne, high-order hold, mixer, RF amplifier, SiGe, single-sideband (SSB), transmitter, wideband code division multiple access (WCDMA).**

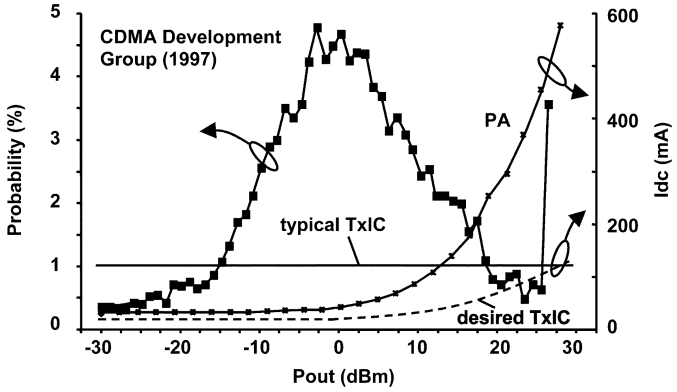

Fig. 1. Current consumption of PA and TxIC versus the transmitter output power, and the output power probability distribution function. A poorly designed TxIC can substantially reduce overall transmitter efficiency.

I. Introduction

THE wireless industry has gradually evolved from originally providing voice service to enabling high-bit-rate communications such as internet access and image and video transfers. Wideband code division multiple access (WCDMA) has emerged as one of the standards within the third-generation (3G) wireless communication framework. Operating as a frequency duplex system, it occupies 1920–1980 MHz for the transmit band and 2110–2170 MHz for the receive band.

As WCDMA gains popularity, there is enormous pressure to reduce the size, cost, and power consumption of the mobile phone. While digital circuits have experienced tremendous power saving and enhanced functionalities with the progress of deep submicrometer processes, the analog/RF sections remain a bottleneck in achieving a low-power high-performance solution. This study focuses on the design of a WCDMA handset transmitter IC (TxIC) with the twin goals of a high level of integration and low power consumption. Located between the digital signal processor (DSP) and the power amplifier (PA), it performs quadrature upconversion of baseband data to the desired transmit channel at the radio frequencies. As shown by the examples in [1]–[10], the TxIC should furnish a wide dynamic range for power control, maintain good waveform quality (as measured by adjacent channel leakage and error vector magnitude), and minimize its spurious emission to avoid desensitizing the nearby receivers operating at a different standard [11].

Existing TxIC solutions commonly require external filters at the intermediate frequency (IF) for spurious rejection. While being a time-proven approach, those off-chip components [for instance, IF surface acoustic wave (SAW) filter, or LC tank] are bulky and expensive. Their successful elimination would substantially reduce the feature size and cost of the final cell phone product. Therefore, it is obvious that a highly integrated TxIC is very desirable. However, one may question the necessity of a low-power TxIC solution, especially in the presence of a presumably far more power-hungry PA. The WCDMA system features a wide dynamic range power control function, to combat the "near–far" problem [12]; when a user is close to the base station, the transmit signal is reduced so that it does not overwhelm the weaker signals from other far away users. Although the PA can consume a high current at the peak output level, the power consumption drops substantially during the power backoff mode (due to its Class AB bias) [13]. This is shown in Fig. 1. Moreover, at the highest probability output power, as shown by the 0-dBm point of Fig. 1, the PA can consume *less* power than a typical TxIC. This makes the TxIC the major determinant of the overall average transmit power efficiency. As a result, a carefully designed low-power TxIC (as shown by the broken line in Fig. 1) is crucial to prolong the battery life.

The highly integrated low-power WCDMA TxIC is achieved through a combination of architecture and circuit innovations. This paper is organized as follows. Section II outlines the improved transmitter architecture based on the digital-IF scheme. Section III describes the low-power circuit design techniques

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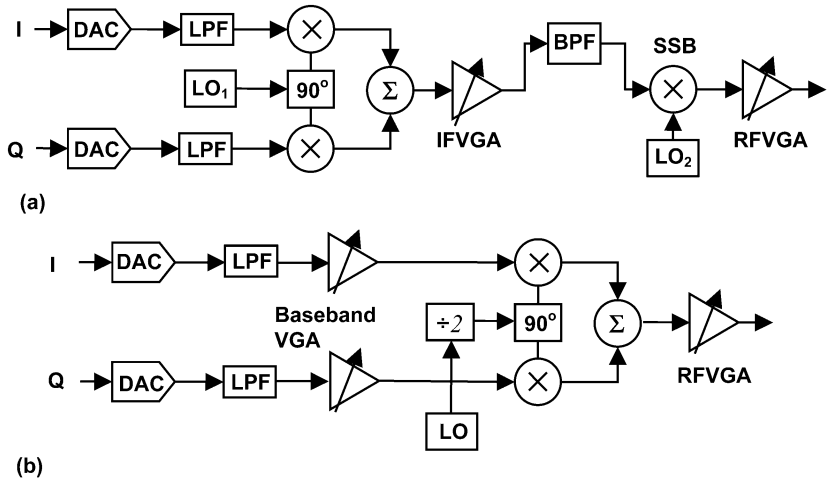

Fig. 2. Conceptual block diagrams of (a) the heterodyne and (b) the homodyne transmitter architecture.

employed for the three TxIC subblocks, namely the digital-to-analog converter (DAC), the single-sideband (SSB) mixer, and the RF variable-gain amplifier (RFVGA). Measurement results are given in Section IV, followed by the summary in Section V.

II. Highly Integrated TxIC Architecture

The majority of WCDMA transmitters reported today are heterodyne [1]–[6]. Performing RF upconversion in two steps as shown in Fig. 2(a), this architecture offers many advantages. Most importantly, the very wide gain control range of 74 dB demanded [11] by the WCDMA standard can be distributed to two VGAs in the IF and RF bands, thus effectively solving the substrate isolation problem. Beside, it is relatively insensitive to local oscillator (LO) leakage. Matching between the in-phase and quadrature-phase (I/Q) signals is excellent, as quadrature modulation is performed at the lower (intermediate) frequencies.

However, as described earlier, the heterodyne architecture often demands external IF filters [1]–[4], thus raising the overall cost and size of the chipset solution. Besides, the architecture demands two sets of synthesizers (at IF and RF) which lead to a complicated and area/ power inefficient design. These drawbacks were recently addressed in [5] and [6], where a variable-IF scheme is employed. However, due to the extended [5] or the high-IF [6] quadrature modulation, the I/Q matching properties will inevitably degrade.

On the other hand, if baseband signals are upconverted to the RF directly, the above issues (namely the external IF filter and multiple synthesizers) could be avoided. The so-called homodyne architecture, shown in Fig. 2(b), lends itself very efficiently to single-chip integration. To avoid LO pulling by the PA output, a divider circuit is employed for LO generation. Also, to overcome the limited substrate isolation at RF, some of the gain control must now be implemented at baseband (dc).

However, the homodyne transmitter suffers performance issues [14], [15] not seen in its heterodyne counterpart. First, the LO leakage will always lie in the transmit band. Additional dc offsets generated in the baseband gain stage, or the attenuated baseband signals, will exacerbate the problem. Second, I/Q mismatches are expected to be more severe as quadrature modulation is performed at RF. These two nonidealities can severely degrade the transmitter error vector magnitude (EVM) performances. To overcome that, the homodyne transmitter of [9] features a carrier leakage cancellation loop, while the design of [10] implements a meticulous gain partitioning and a variable LO (reduced LO for small signals).

An ideal transmitter should be one that exhibits the architectural simplicity of the homodyne (that is, it demands no external IF filter and only one synthesizer), but inherits the performance advantages of the heterodyne (that is, it provides superior I/Q matching and produces little LO leakage for good EVM performance). The WCDMA transmitter to be presented below is a unique attempt to simultaneously satisfy these goals.

Based on the conventional heterodyne design, our proposed WCDMA transmitter features a *digital* IF modulator, as shown in Fig. 3 [16]. Digital data (at 3.84 MHz chip rate) are upsampled (interpolated), filtered, multiplied with the quadrature LOs, and then summed together before application to the (single) digital-to-analog converter (DAC). To simplify the design of the digital quadrature modulator, we impose the condition: $f_{\rm IF} = f_{\rm clk}/4$ (the IF is equal to a quarter of the DAC clock rate). As a result, the quadrature LOs will only take on values of $+1$, 0, or -1, and multiplication is a simple sign-bit-flipping/ zeroing logic. Therefore, there is no need for a full-function N-bit digital multiplier or a numerical oscillator.

This solution demands only one RF synthesizer and mixer to complete the upconversion. The DAC clock will be derived from the phase-locked loop (PLL) on the digital baseband chip. As the digital boundary is moved closer to the antenna, this architecture will take full advantage of silicon technology scaling. Furthermore, since modulation is performed digitally, and there are no separate analog baseband I/Q paths, near-ideal I/Q matching and enhanced EVM performance will result. LO leakage is a relatively minor issue here, as it will not overlap with the transmit channel. Moreover, ac coupling can be routinely applied to cancel any dc offset on the analog circuits (as there is no signal content at dc).

Despite these well-known advantages, traditional digital-IF approaches usually exhibit high power dissipation and are better

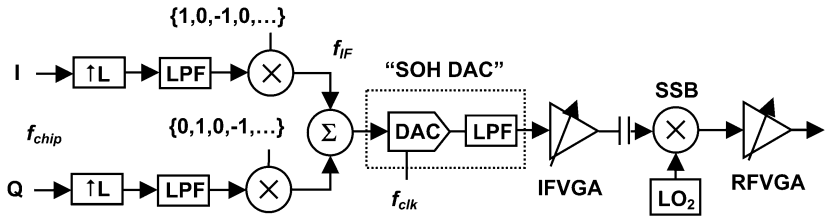

Fig. 3. Conceptual block diagram of the digital-IF heterodyne transmitter.

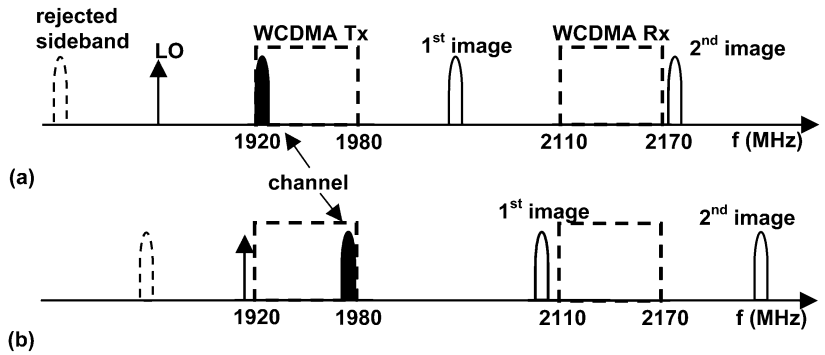

Fig. 4. Frequency planning illustration: locations of images when the channel is at (a) the lower or (b) the upper edge of the WCDMA Tx band. Images will always skip the forbidden Tx and Rx bands, thus substantially relaxing the filter requirements.

suited to base-station applications. Here, two architecture features [16] were derived to yield a simple, highly integrated (with no off-chip IF filter) low-power solution suitable for a WCDMA handset.

First, if the clock is selected strategically so that the DAC images will always appear out of the frequency bands of interest [such as the WCDMA transmit (Tx) and receive (Rx) bands] for all channel locations, the IF filter requirements could be substantially relaxed. This frequency plan is shown in Fig. 4. Our analysis shows that this could be satisfied if the DAC clock rate is set to be between 250–260 MHz [16]. For an integer upsampling ratio of 66 ($L = 66$, Fig. 3), the DAC clock and the IF frequencies are selected to be 253.44 and 63.36 MHz, respectively.

Second, instead of filtering the spurious outputs, we implement a DAC that reduces image generation in the first place. Traditional zeroth-order-hold (ZOH) DACs produce sample-and-hold (S/H) waveforms and attenuate the images with the slow $\sin(x)/x$ response. If the DAC produces "ramp" outputs [or a "first-order-hold" (FOH) reconstruction], the images will roll off at the elevated rate of $(\sin(x)/x)^2$, as shown in Fig. 5.

The implementation of a FOH DAC is similar to a conventional current-steering DAC, as shown in Fig. 6. A current is generated which is proportional to the *difference* between two consecutive input digital codes (digital differentiation), then the current is delivered to a *capacitor* to perform the I-to-V conversion (analog integration). The FOH DAC signal processing can be further generalized to yield a Kth-order-hold DAC, where a $(\sin(x)/x)^{K+1}$ response is implemented by cascading K digital differentiators and K analog integrators. This concept is potentially useful for any D/A conversion applications, as long as the signal of interest is passband (no dc content) in nature. (one example is digital-IF). This is because the high-order-hold DAC experiences a singularity at dc, where infinite attenuation of the digital differentiators is greeted by infinite amplification of the analog integrators.

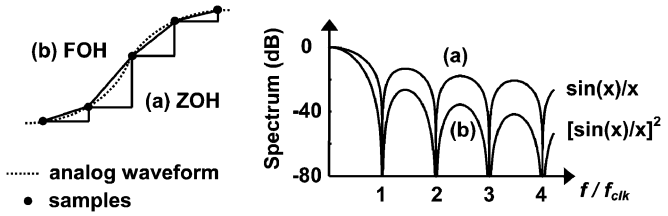

Fig. 5. Transient waveforms of (a) the ZOH (S/H) DAC and (b) the FOH DAC and their corresponding spectrum rolloffs.

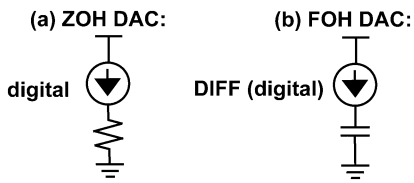

Fig. 6. Conceptual implementations of (a) the (conventional) current-steering ZOH DAC and (b) the FOH DAC. They are very comparable.

Simulations show that, when a second-order-hold (SOH, $K = 2$) DAC is employed, the WCDMA spurious emission requirements are met with *no* dedicated reconstruction filter [16]. Fig. 7 displays the final TxIC architecture. Resolution of 8-b is selected for the DAC to satisfy the spectral emission mask [17]. The two analog integrators associated with the SOH DAC are naturally incorporated into the DAC core and the IF VGA (IFVGA). A gain control range of 90 dB will be implemented, which is equally distributed between the IFVGA, the SSB mixer, and the RFVGA.

In summary, the digital-IF transmitter, with the help of the frequency planning and the high-order-hold DAC, achieves the architectural simplicity of a homodyne while exhibiting the performance advantages of the heterodyne.

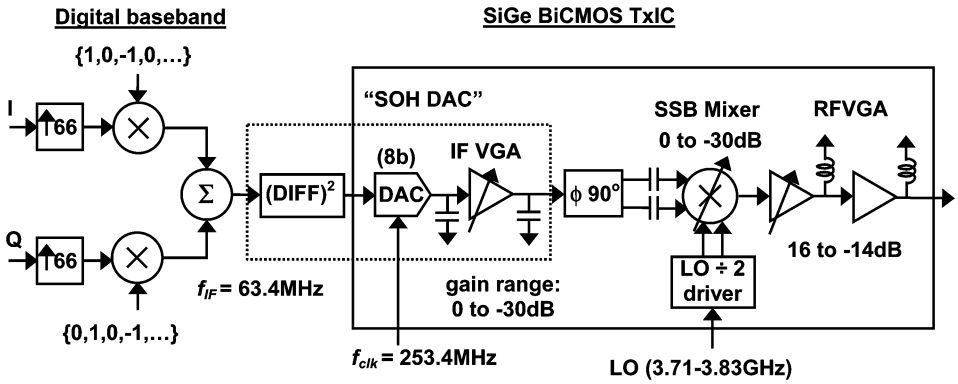

Fig. 7. Proposed digital-IF TxIC architecture. Employing the optimized frequency plan and the SOH DAC, spurious emission requirements are met with no dedicated IF filters.

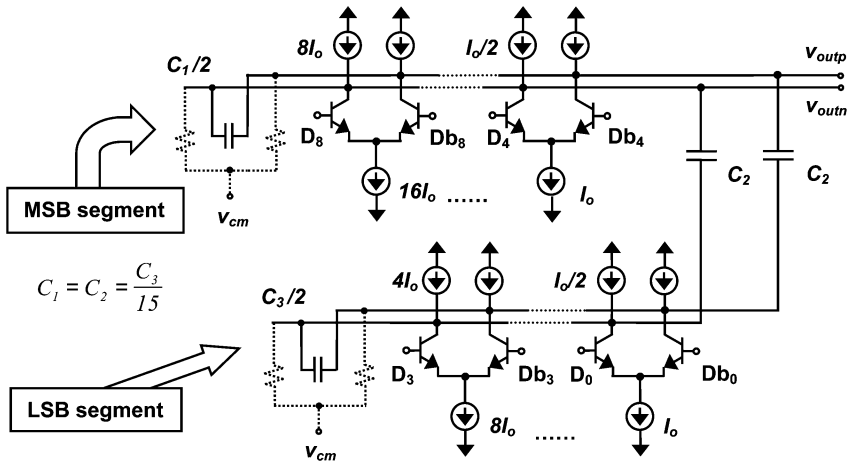

Fig. 8. Simplified schematic of the SOH DAC core, featuring the dominantly capacitive load.

III. Low-Power TxIC Circuits

A. 8-b 250-MHz SOH DAC

The 250-MHz SOH DAC includes an 8-b current-steering architecture with a dominantly capacitive load. Fig. 8 shows the DAC core. The fast bipolar npn switches available in the SiGe BiCMOS process allow high-speed conversion (high f_T) at very low bias current—a key issue with digital-IF approaches. The switches are scaled with respect to the current source values to minimize the effects of the parasitic base–collector capacitances.

Note that current sources and sinks are employed both above and below the switches. This is done so that, depending on the differential digital inputs, binary-weighted currents can be steered into and out of the capacitors, thus effectively performing charging or discharging.

The common-mode output voltage is set by a pair of relatively large resistors (around 2 kΩ), which also damp the otherwise ideal integrator and prevent it from saturating. Mismatch between the top and the bottom current sources only produces a finite dc offset voltage. Since the dc offset would be subsequently eliminated by ac coupling, it has no effect on the (bandpass) IF signal as long as no transistor is forced out of its normal mode of operation. In this regard, we have budgeted 200 mV of tolerable offset voltage, corresponding to the relaxed matching requirement of 100 μA between the top and the bottom current sources.

Due to the digital second-order differentiation prior to the DAC (see Fig. 7), one additional bit will be generated. So, there are a total of nine input bits for the 8-b D/A conversion. A straightforward implementation would demand nine binary-weighted current stages or a current mirror ratio of 256 to 1. This is rather impractical from a current source matching perspective and translates to high current consumption. Assuming that the LSB current (I_o) can be as low as 50 μA (so that $f_T = 20$ GHz is achieved for the minimum-sized pedestal device in the advanced SiGe BiCMOS process), the MSB current would equal 12.8 mA. The total current consumption would sum to 25.6 mA.

To reduce the mirror ratio and therefore the power consumption, we employ a simple capacitor current divider. Fig. 9 shows the single-ended conceptual diagram. We divide the current $(I_{\rm LSB})$ coming from the lower LSB segment (last 4-b) by 16, and sum it with the upper segment (upper 5-b) current, $I_{\rm MSB}$. Assuming that $C_1 = C_2 = C$, the output voltage due to $I_{\rm LSB}$ (when $I_{\rm LSB} = I$ and $I_{\rm MSB} = 0$) equals

$$\nu_{\rm out,LSB} = \frac{I}{2} \bullet \left[\frac{2}{sC} // \frac{1}{sC_3} \right]. \tag{1}$$

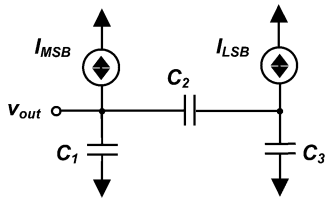

Fig. 9. Single-ended conceptual diagram of the 16-to-1 capacitor divider network.

On the other hand, the output voltage due to $I_{\rm MSB}$ (when $I_{\rm LSB} = 0$ and $I_{\rm MSB} = I$) equals

$$\nu_{\rm out,MSB} = \frac{I}{2} \bullet \left[\frac{1}{sC} // \frac{C + C_3}{sC \bullet C_3} \right]. \tag{2}$$

To perform the 16-to-1 current division, we require that $\nu_{\rm out,MSB} = 16 \bullet \nu_{\rm out,LSB}$. We can solve for C_3 from (1) and (2) and find $C_3 = 15 \bullet C$.

With this simple capacitor divider network, as shown in Fig. 8, the lower (LSB) segment is composed of current sources of values: $\{I_o, 2I_o, 4I_o, 8I_o\}$, while the upper (MSB) segment takes on values of $\{I_o, 2I_o, 4I_o, 8I_o, 16I_o\}$. As such, the ratio of the largest-to-smallest current is reduced from $256:1$ to $16:1$. With the minimum LSB current (I_o) of 50 μA, the DAC core consumes only 2.3 mA, which is less than one tenth of what would be otherwise required.

Of course, close attention must now also be paid to the matching between the capacitors (in addition to the matching between the bottom current sources). However, since only 8-b of resolution is targeted in the transmitter architecture, the issue is not expected to be insurmountable.

Since I–V conversion is carried out by capacitor integration, the output signal amplitude is a function of LSB bias current (I_o), total load capacitance $(C_{\rm load} \simeq C_1 + C_2)$, as well as the signal frequency $(\omega_{\rm IF} = 2\pi f_{\rm IF})$ and the clock period $(T_{\rm clk} = 1/f_{\rm clk})$:

$$v_{\rm out,ppd} = 4 \bullet \frac{(16I_0) \bullet T_{\rm clk}}{C_{\rm load}} \bullet \frac{1}{|1 - e^{-j\omega_{\rm IF} T_{\rm clk}}|}. \tag{3}$$

To make the DAC less susceptible to glitches and clock feedthrough, it is designed to handle a maximum of 1 $V_{\rm ppd}$ output. With $I_o = 50$ μA, $f_{\rm IF} = 63.36$ MHz and $f_{\rm clk} = 253.44$MHz, the total capacitance $C_{\rm load}$ is found to be approximately 8 pF according to (3). Therefore, we have $C_1 = C_2 = C_3/15 = 4$ pF. To ensure good element matching, common-centroid layout techniques are employed for the capacitor array as well as the bottom current source array.

For good dynamic (high-speed) performance, CMOS latches and switch drivers [18] are designed to synchronize data on-chip and convert digital logic levels into differential switch driving signals. They are optimized for symmetric and fast switching (within 200 ps) to minimize harmonic tones in the output spectrum.

The IFVGA circuit is shown in Fig. 10 and provides the second analog integration for the SOH D/A conversion. Input

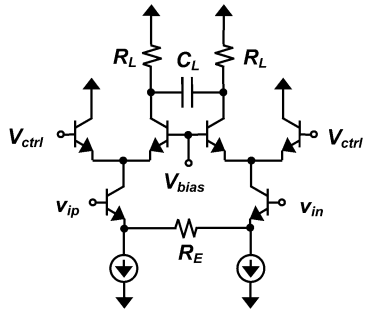

Fig. 10. Schematic of the IFVGA. It implements the second integrator for the SOH D/A conversion.

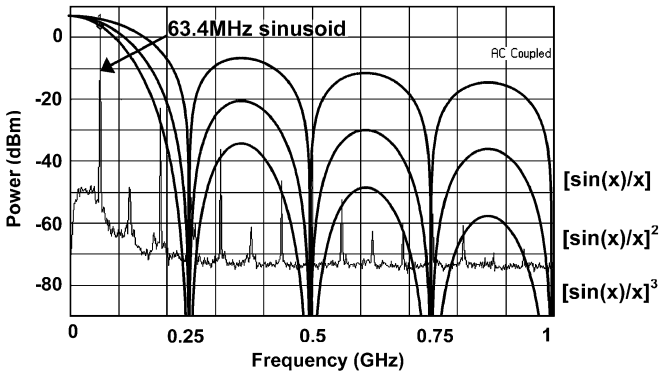

Fig. 11. Measured SOH DAC output spectrum from dc to 1 GHz. It exhibits the elevated $[\sin(x)/x]^3$ image roll-off.

voltages (from the DAC) are applied to the differential pair with emitter degeneration, while load resistors are present at the collectors of the cascode devices. (Variable gain is achieved by adjusting $V_{\rm ctrl}$ versus $V_{\rm bias}$.) To turn the amplifier into a (damped) integrator, a capacitor C_L is connected across the output nodes to form a pole below the signal frequency. The IFVGA frequency response is given by

$$H(s)_{\rm IFVGA} = \frac{\dfrac{2R_L}{R_E}}{I + s(2C_L R_L)}. \tag{4}$$

The SOH DAC subsystem (which also includes IFVGA/ integrator) consumes a total of 8 mA with a 3-V supply. The measured DAC output spectrum (from dc to 1 GHz) for a full-scale single-tone sine wave at 63.4 MHz (or a quarter of the clock rate of 253.4 MHz) is shown in Fig. 11. It exhibits the elevated $(\sin(x)/x)^3$ roll-off, thus confirming the SOH DAC behavior and satisfying the WCDMA spurious requirements.

To demonstrate the DAC high-speed performance, the spurious-free dynamic range (SFDR) is measured to be 54.5 dB, as shown in Fig. 12. The third-order intermodulation distortion ratio $(\rm IMR_3)$ is measured to be -50 dB, while the WCDMA adjacent channel power rejection (ACPR) is measured to be -44 dB. We believe that the dynamic performances are limited partially by the segmented binary-weighted architecture (which tends to produce higher glitch energy) and the switch driver design.

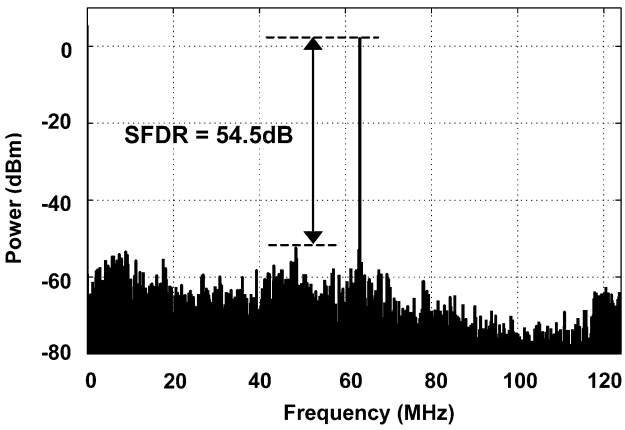

Fig. 12. Measured SFDR of the SOH DAC.

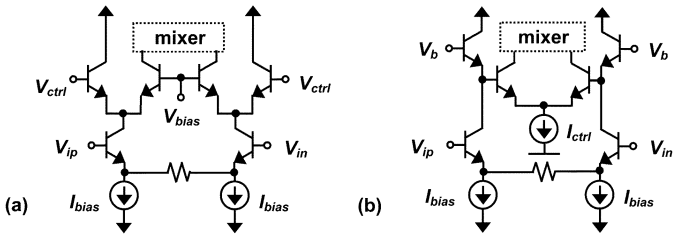

Fig. 13. Implementation of mixer variable-gain through (a) a bleeder circuit and (b) a translinear stage. The translinear circuit is more power-efficient as current consumption will drop with the mixer gain simultaneously.

B. SSB Mixer

To perform single-sideband upconversion, in-phase (I) and quadrature-phase (Q) signals must be generated from the single IF input at 63.36 MHz. This is accomplished by a 90° broadband phase-shifting network [19]. Besides, quadrature LO signals are also generated from a single off-chip LO input (at two times the desired frequency). This is accomplished by a divide-by-two buffer circuit, in which two latches are connected in a negative feedback loop [20]. The inevitable I/Q imbalance introduced by these two circuits will cause a residual (not perfectly rejected) lower sideband. Since the residual sideband will cause no degradation to EVM performance, it is generally tolerable as long as the spurious emission requirement is not violated.

In a conventional heterodyne transmitter, where the IF is at 380 MHz [1]–[4], the variable-gain mixer typically involves the use of current-steering cascode devices (bleeder), as shown in Fig. 13(a). Similar to the IFVGA, gain control is achieved by raising $V_{\rm ctrl}$ relative to the $V_{\rm bias}$. While being very reliable for high-speed applications, the structure is rather wasteful, as constant power is consumed for all output levels. Instead of reducing the current consumption at lower gain, a large amount of valuable bias current is simply discarded.

In our case, with a relatively low IF of 63.4 MHz, the variable-gain mixer can be efficiently achieved with a translinear input stage [21], as shown in Fig. 13(b), where the gain is dictated by the *current* ratio $I_{\rm ctrl}/I_{\rm bias}$. Gain control can then be achieved by reducing the current $I_{\rm ctrl}$ versus a constant $I_{\rm bias}$, so that the power consumption will decrease for reduced mixer gains. This characteristic is crucial as the average efficiency (not only the peak efficiency, but the efficiency evaluated over a wide range of statistically distributed output levels) can be optimized.

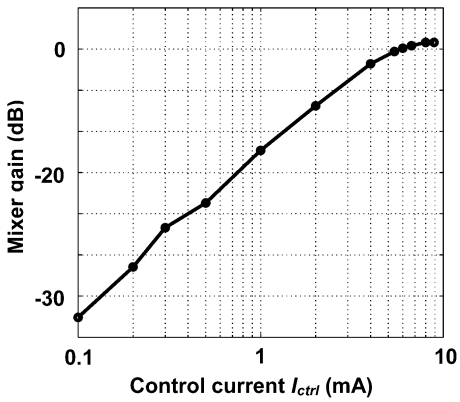

Fig. 14. Measured mixer gain versus the control current $(I_{\rm ctrl})$.

To achieve more than 30 dB of gain programmability, $I_{\rm ctrl}$ is reduced from 8 mA to 100 μA (where $I_{\rm bias} = 1$ mA). Fig. 14 shows the measured mixer gain versus the control current. The total SSB mixer current consumption reduces from 30 mA (high gain) to 14 mA (low gain), which translates to a substantial 50% power savings for reduced gain.

C. RFVGA

The RFVGA is a two-stage design shown in Fig. 15. The first stage features a cascode amplifier, whose gain control is conducted in a similar manner as the IFVGA. The second stage is a common-emitter (CE) amplifier. The output network is designed for power matching to a 50-Ω load. The key is to keep the quiescent current for both stages as low as possible using "smart" adaptive bias schemes [22] and allow the amplifier to achieve higher average current *only* when needed (Class AB bias).

To that end, the CE amplifier features a constant (base) voltage bias through an active buffer circuit, which supplies additional base current at a high-output power level for (Class AB action). Similar to the conventional floating inductor base bias, the buffer presents a high impedance at 2 GHz and a near-zero impedance at dc. At the expense of very small power consumption, it consumes much smaller silicon area than an on-chip inductor and introduces far less capacitive coupling between the RF input and the substrate.

Note that, for the cascode amplifier, a resistor (instead of an inductor) emitter degeneration is employed as shown in Fig. 15. While this saves tremendous silicon area, the resistor renders the constant-voltage bias ineffective, since it would compress the base-emitter voltage as soon as the average collector current rises, thus severely limiting the Class AB action.

To mitigate this, we employed an adaptive bias control technique, based on the power detector circuit shown in Fig. 16. Power detection is accomplished by two bipolar devices (Q_1, Q_2) configured as CE amplifiers. They are biased with low quiescent current (I_{cq}), and their collector currents will be clipped during large-signal conditions. As a result, their average (dc) collector currents will be raised above the quiescent level. The extra dc current, which is proportional to the input power, will be mirrored and multiplied (with a digitally programmable ratio by transistor pair M_3–M_4). Eventually, it will be applied to supplement the fixed quiescent current $(I_{\rm cq1})$ of the cascode amplifier bias network of Fig. 15.

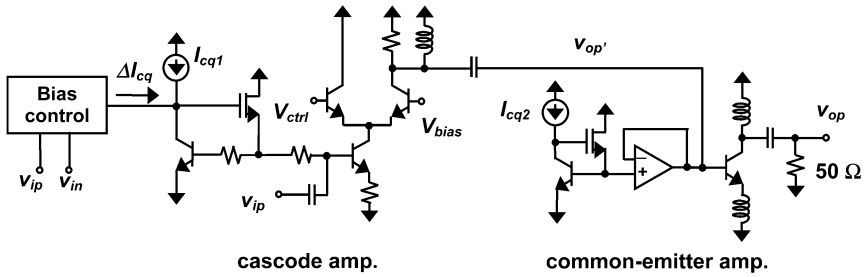

Fig. 15. Simplified schematic of the RFVGA. The two-stage design features adaptive bias schemes to make linearity requirements while minimizing the quiescent current consumptions.

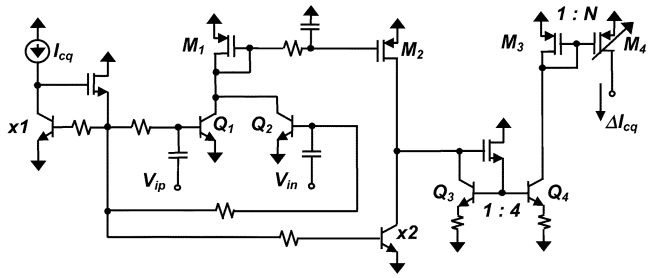

Fig. 16. Power-detector bias-control circuit.

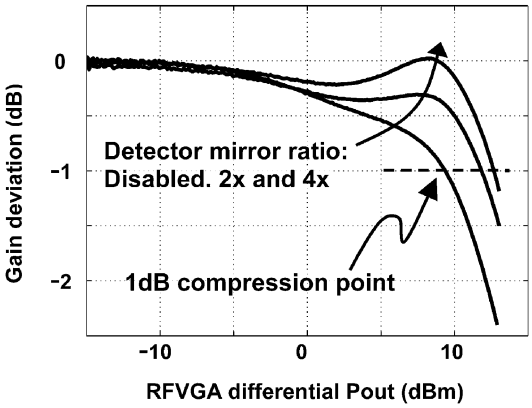

Fig. 17. Measured gain compression of the RFVGA versus output power level. Due to the current boost, gain compression is compensated for by gain expansion, thus increasing the 1-dB compression point by 3.5 dB.

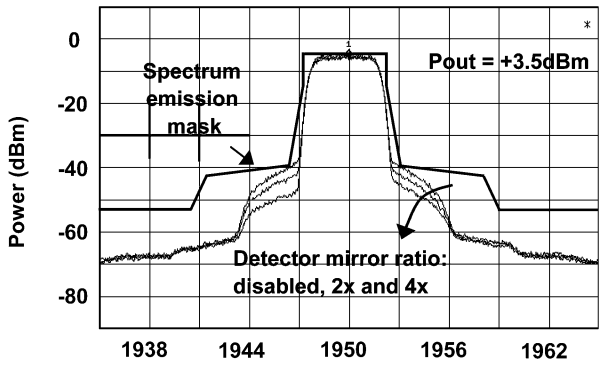

Fig. 18. Measured ACPR of RFVGA showing the linearity improvements due to the power-detector bias control.

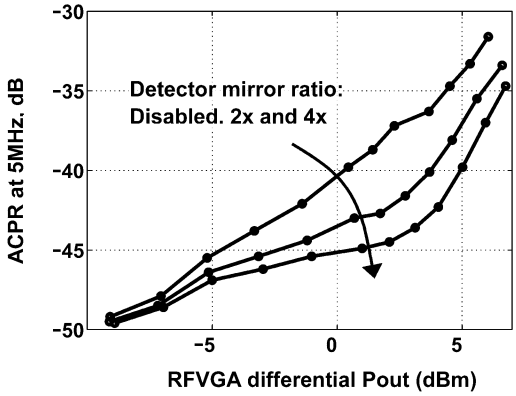

Fig. 19. Measured RFVGA ACPR results versus output power. Linearity improvement is observed over a wide range of power level.

The measured RFVGA gain is 16 dB. It consumes a total quiescent current of 9 mA with a 2.7-V supply. The quiescent power saving is about 60% versus a simple Class A design. Fig. 17 shows the resulting gain compression versus output power. Due to the dynamic bias (current boost at high power), gain *compression* is compensated by gain *expansion*, resulting in enhanced dynamic range *without an increase in quiescent dc power*. The output 1-dB compression point is increased from +9.2 dBm to +12.7 dBm, an improvement of 3.5 dB.

The dynamic bias also improves the RFVGA linearity, as shown in Fig. 18. At the (maximum) WCDMA power level of +3.5 dBm, the detector circuit has improved the ACPR by 6 dB. The ACPRs at 5 and 10 MHz equal −43 and −59 dB, respectively. The measured ACPR (at 5-MHz offset) versus the output power is plotted in Fig. 19. Linearity improvement is achieved over a wide range (10 dB) of output levels. For small-signal power (where the amplifier linearity is acceptable without the current boost), the detector circuit does not respond. Maximum ACPR improvements are then attained near the amplifier maximum average output level. Moderate improvement is still achieved when the signal power approaches the amplifier 1-dB compression point.

IV. Measured TxIC Results

The TxIC chip is fabricated in IBM's 0.25-μm SiGe BiCMOS process [23], and it is shown in Fig. 20. It incorporates the SOH DAC, the SSB mixer, and the RFVGA circuits (see the chip boundary[1] in the transmitter architecture diagram of Fig. 7). The chip contains six inductors, 400 capacitors, 320 npns, and measures 1.8×2.2 mm^2 including the pads.

[1]To establish the validity of the architecture and to demonstrate the low-power consumption of analog frontend circuits, we have decided to integrate only the core mixed-signal and RF components. The digital parts, such as the interpolators, the modulators, and the differentiators are omitted for simplicity.

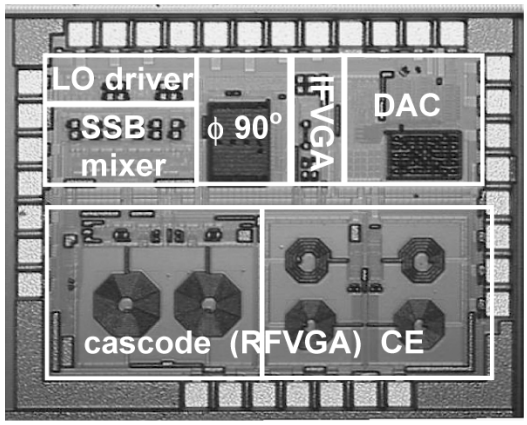

Fig. 20. TxIC chip microphotograph. It measures 1.8×2.2 mm^2.

Fig. 21(a) shows the measured TxIC output spectrum in the digital cellular system (DCS)/ WCDMA Tx and Rx bands. A channel is being transmitted in the middle of the Tx band at 1950 MHz. With resolution bandwidth (RBW) of the spectrum analyzer set to 3 kHz, the channel power is measured to be $+5.5$ dBm integrated over the occupied bandwidth of 4 MHz. Notice that the spurious emissions, which include the residual (lower) sideband, LO leakage, digital images, and the (DAC) clock feedthrough, will be further reduced by the external filters (namely the RF SAW and the duplexer[2]) before they reach the antenna.

We then normalize and express the measured TxIC spectrum in dBc/5 MHz and include the additional external filter attenuation. The results are shown in Fig. 21(b). The spurious emission requirements at different regions are also superimposed [11]. This represents the worst-case scenario as the TxIC is operated at its peak output power (while the spurious emissions are specified in absolute terms). The spurious emission requirements are met in various regions, except for a few performance issues which will be addressed below.

Due to the imperfect high-speed data and clock alignment at the DAC input, excess noise is being injected to the input. This noise is amplified by the double integrators (of the DAC core and the IFVGA), thus resulting in the tilted Tx noise floor, as observed in Fig. 21, which slightly exceeds the spurious requirements around 1920 MHz. Furthermore, the injection of noise also creates a relatively high noise content at the Rx band (2110–2170 MHz). In theory, the quantization noise should be substantially rejected in the middle of the Rx band due to the notch of the $\sin(x)/x$ rolloff [16]; the notch is partially "filled up" by the noise injection. An improved data latch design and a more balanced layout (for the clock and input signals at the board and the chip levels) will mitigate this issue.

When WCDMA channel is located at the lower end of the transmit band (1920 MHz), the LO leakage would move into the DCS Rx frequencies. In this chip version, only 30 dBc of LO rejection is measured, which can violate the spurious emission

[2]In this analysis, the RF SAW filter is selected to be SAWTEK 855938, while the duplexer is CTS Wireless Components KFF6669A. Of particular concern is the attenuation at the DCS Rx band (1805 to 1880 MHz) where, depending on the channel location, the LO leakage and/or the undesired sideband will appear. Together the filters will give approximately 35 dB of attenuation in that region

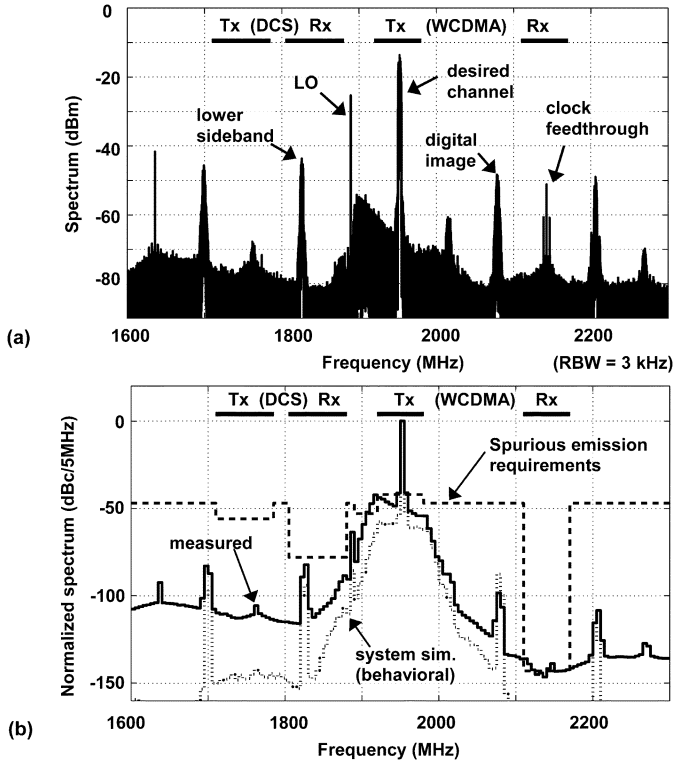

Fig. 21. (a) The measured TxIC output spectrum in the DCS and WCDMA bands (resolution bandwidth equals 3 kHz). (b) Normalized and including the external filter attenuation, it is shown to meet the spurious emission requirements.

requirements in the DCS Rx region. This can be mitigated if the LO rejection is increased to 40 dBc, which can be practically achieved by a more balanced layout.

On the other hand, the undesired sideband would be least attenuated (by the external filters) when the channel is at the upper edge of the transmit band (1980 MHz). With the measured 35-dBc sideband rejection, the spurious requirements on the DCS Rx band can be violated. An improved sideband rejection of 40 dBc would resolve this issue, which can be accomplished by ensuring more precise quadrature (I/Q) IF and LO signals.

Notice that, when generating Fig. 21(b), PA nonlinearities are not included. In reality, when the spurs are applied to the PA together with the desired signal, additional intermodulation products can be generated and potentially fall into susceptible frequency bands. However, we believe that since the spurs are of relatively small amplitude (more than 30 dB below the channel), this issue should not be the limiting factor. Nevertheless, caution should be exercised during system integration.

Fig. 22 displays the measured LO and sideband leakage versus the TxIC gain control. At the maximum output power, they are measured to be 30.5 and 35 dBc, respectively, and remain at that level for a wide (50 dB) range.

Fig. 23 shows the measured TxIC ACPR versus gain control. The ACPR at 5- and 10-MHz offsets are measured to be -42 and -51 dBc, respectively, at the maximum output power. They meet the WCDMA specifications of -33 and -43 dBc with good margins. In this measurement, the true distortion is lower

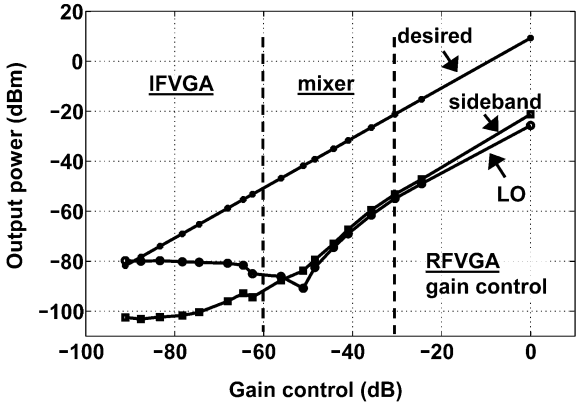

Fig. 22. Measured TxIC residual sideband and LO leakage.

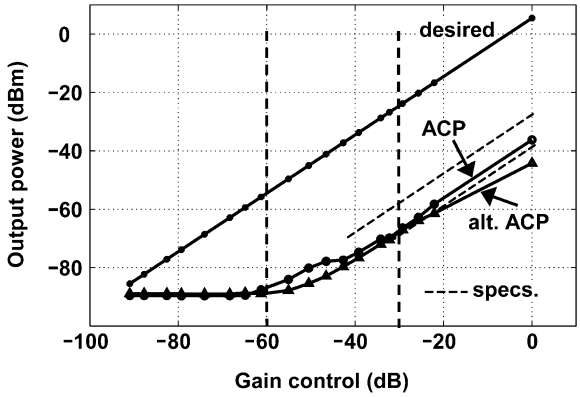

Fig. 23. Measured TxIC ACPRs.

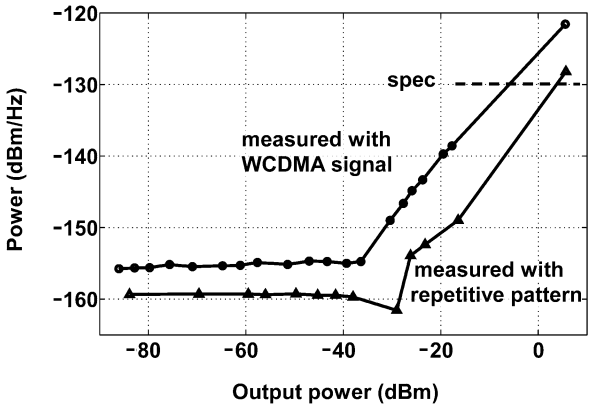

Fig. 24. Measured TxIC noise in the WCDMA Rx band.

than these results and is masked by the tilted transmit band noise as described earlier.

Fig. 24 shows the measured TxIC noise in the Rx band versus gain control. Measured with a WCDMA signal, the worst-case noise in the Rx band is measured to be −121 dBm/Hz, which is relatively high compared to the typical specification of −130 dBm/Hz. As demonstrated by running the following experiment, it can be shown that the high noise floor is dominated by the DAC quantization noise. When a simple repetitive digital pattern (such as 00 110 011…) is applied to the TxIC, the DAC quantization noise can be effectively "turned off." In that case,

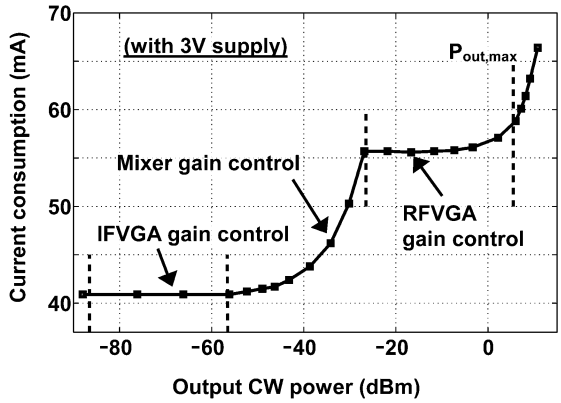

Fig. 25. Measured TxIC current consumption. It exhibits substantial power savings for power backoff mode.

the noise reduces to −128 dBm/Hz. It reflects the true thermal or circuit noise and is more comparable to other state-of-the-art solutions [4], [6], [10]. The relatively high quantization noise floor can be easily reduced by adding an extra pole to the IFVGA, if necessary.

Finally, Fig. 25 presents the TxIC current consumption versus the output power. The TxIC exhibits a substantial drop of current consumption at reduced output power, which is highly desirable as pointed out in the Introduction. At a 3-V supply, the TxIC consumes 180 mW at the maximum average power and 120 mW at the minimum output level.[3]

The full version of this digital-IF TxIC chip would integrate the digital baseband functions (such as upsampling, IF upconversion, and digital differentiation) as well as the RF frequency synthesizer. This would give a more definite picture on the overall power and silicon area consumption. Besides, it would provide valuable insights on, given all the isolation techniques supported by the SiGe process, the level of digital noise coupling to the sensitive analog/ RF circuits in this heavily mixed-signal environment.

The summary of the measured TxIC performances is shown in Table I. The measured EVM is less than 1%. This excellent EVM performance should be compared to the state-of-the-art solutions that report 2.5%–6% [1], [2], [4], [6], [7]. While this good EVM result may be an overkill for WCDMA system, which features relatively simple signal constellation and a limited crest factor, it indeed demonstrates the unique characteristic of the digital-IF scheme. It will become an even more significant advantage when the architecture is attempted for a system (such as the OFDM-based WLAN systems) where more stringent EVM requirements are demanded.

The TxIC of this study is compared to other published WCDMA TxIC designs [1]–[10], as shown in Table II. In terms of the level of integration, this work exhibits the simplicity of a homodyne architecture: it demands no external image-reject

[3]To complete the picture, we should also estimate the power consumed by the digital portion of the transmitter architecture. Implemented on a field-programmable gate array (FPGA), the 66 × interpolation of Fig. 7 employs a multistage polyphase architecture [24]. Approximately 100 K gates are employed, of which 22% run at 7.7 MHz, 20% at 23 MHz, and 60% at 69 MHz. If this gate count is directly translated to a 0.15-μm CMOS ASIC implementation, approximately 40 mW of digital power consumption will result

TABLE I
SUMMARY OF MEASURED TXIC PERFORMANCE

Parameter	Measured
Supply (V)	3.0
DC current (mA)	41–58
Carrier supp. (dBc)	-35
Sideband supp. (dBc)	-30.5
QPSK EVM (%rms)	<1%
CW Pout (dBm)	+9.3
WCDMA Pout (dBm)	+5.5
Dynamic range (dB)	90
OIP3 (dBm)	+16
Occup. BW (MHz)	4.18

Parameter	Measured
ACPR (dBc)	-42 (5MHz)
	-51 (10MHz)
Tx noise (dBm/5MHz)	-48.7 (typical)
	-38.6 (worst)
	-59.5 (no $N_{Quantz.}$)
	-86.8 (min)
Rx noise (dBm/Hz)	-121.6 (max)
	-128.2 (no $N_{Quantz.}$)
	-155.8 (min)
clk_{fdthru} (dBm)	-53

TABLE II
COMPARISON OF PUBLISHED WCDMA TXIC WORK

Company/ Institutions	Arch.	External IF/ IRF?	Num. Analog mix/syn	Gain Range (dB)	Integrated components	Max. Pout (dBm)	Power Consump.
Mitsubishi [1]	Hetero.	Y / Y	2 / 2	100	IF + RF	+7	97mA (3V)
IBM [2]		Y / Y	2 / 2	95	IF + RF	+7	90mA (3V)
Mitsubishi [3]		Y / Y	2 / 2	100	IF + RF, with 2 syn.	+7	63–84mA (3V)
TI [4]		Y / N	2 / 2	90	IF + RF, with 2 syn.	+6	67–79mA (2.7V)
Philips [5]	Hetero. var. IF	N / N	2 / 1	81	IF + RF, with 1 syn.	+5.5	81–124mA (2.6V)
IBM [6]		N / N	2 / 1	115	IF + RF	+6.2	100mA (2.85V)
Swiss ETH [7]	Homo.	N / N	1 / 1	78	RF (no PA driver)	-8	40.5mA (2.5V)
Seoul Nat. U. [8]		N / N	1 / 1	50	RF, with syn. & DAC	+6	110mA (3.3V)
Swiss ETH [9]		N / N	1 / 1	100	RF	+2.5	45mA (1.5V)
Qualcomm [10]		N / N	1 / 1	90	RF, with synthesizer	+10	71mA (2.7V)
UCSD (this work)	Hetero. dig. IF	N / N	1 / 1	90	RF, with DAC	+5.5	40–60mA (3V)

filter[4] (IRF) or IF filter and requires a single analog mixer and synthesizer. In addition, this TxIC is among the most power-efficient. Although no synthesizer is included, the TxIC has uniquely integrated the high-speed DAC and the associated filtering functions. It also features one of the most aggressive power-reduction schemes for the power backoff mode.

V. SUMMARY

Based on the digital-IF scheme, a highly integrated TxIC in 0.25-μm SiGe BiCMOS is developed for WCDMA mobile phone applications. It offers the simplicity of the homodyne architecture with the performance benefits of the heterodyne. Optimum frequency plan and SOH DAC are employed to mitigate the high power consumption and the complicated filtering issues typically associated with the digital-IF interface. It achieves substantial power savings at reduced output power through adaptive bias control in the mixer and the RFVGA. This TxIC architecture, whose D/A boundary is moved aggressively toward the antenna, will benefit fully from future technology migration.

[4]The IRF is the external RF filter that follows the upconversion mixer for sideband removal. It is required for the heterodyne transmitter if a single-sideband mixer is not implemented.

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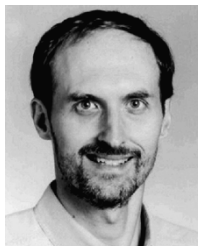

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