An 8bit 3GHz Si/SiGe HBT Sample-and-Hold

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Abstract— **An 8bit 3GHz HBT sample-and-hold amplifier is demonstrated in a 0.5μ m, 55GHz Si/SiGe HBT technology. The SHA core consumed 90mA from an 8 volt supply.**

I. Introduction

Next-generation millimeter-wave fixed wireless internet systems will require low-cost, high-bandwidth receivers operating in the 20-70GHz range [1]. The intermediate frequency (IF) of the receiver chain is often in the 2-4GHz range, and so a second down-conversion step is usually required. One possible approach employs direct digital bandpass sampling of the IF signal, as shown in Fig. 1. The sample-and-hold has the most exacting requirements on linearity for the analog-to-digital converter, in addition to the extremely wide bandwidth requirements.

The increasing bandwidths of these systems put a greater demand on the digital conversion of the received signal; the analog-to-digital-converter (ADC) must operate at a higher sampling rate, while still maintaining a large signal-to-noise-and-distortion ratio. High-frequency, Multi-stage ADCs require a sample-and-hold amplifier (SHA), whose performance sets the overall performance of the system. It is important that the sample-and-hold introduce very little in-band distortion since distortion incurred in the analog portion of an ADC is difficult to remove by subsequent digital correction.

This paper presents an analysis of a switched-emitter-follower based sample-and-hold, along with improved circuit design techniques to minimize the high frequency sampling errors. The bandwidth and dynamic range of this circuit at the required sample rate is superior to other SHA's in silicon technology, see Table I.

II. Track-and-Hold Architecture

The SHA must have a bandwidth greater than that of the maximum expected input signal and it must settle to the specified accuracy in a short amount of time, usually much less than half a clock cycle. Our SHA was designed to precede a moderate resolution, but high sample-rate ADC (5-6bit).

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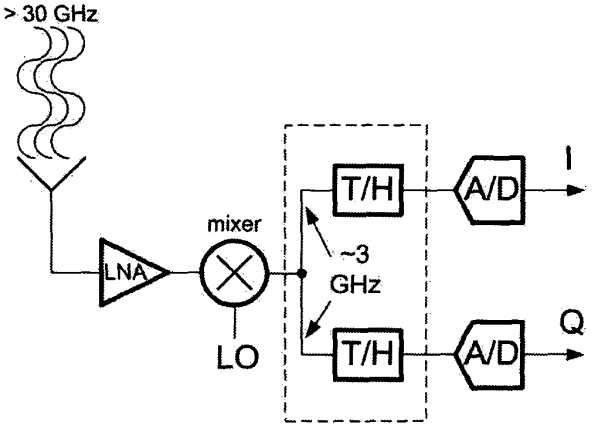

Fig. 1. High frequency receiver with digital bandpass I/Q down converter.

Switched-emitter followers, SEF, were used as the starting point for our design [2,3] (see Fig. 2). Each THA is comprised of unity-gain buffers followed by switched emitter-followers that capture the input signal onto the hold capacitor. Compensation capacitors, C_{comp}, are connected from the negative input node to the positive output node, and vice versa, to decrease signal feed-through during the hold phase [2]. In order to reduce the magnitude of the common-mode signal the output buffer remained "on" during the hold phase. This slightly increased the common-mode droop rate, but also greatly reduced the common-mode swing at the output. Cascode devices, not shown in the simplified figure, were placed between the clock signal and the switched emitter-follower to reduce the clock injection onto the held signal.

A. Switched Emitter-Follower Distortion

This SHA is comprised of three parts: a highly linear, degenerated, differential input pair, Q_1 and Q_2; a pair of switched-emitter followers, Q_3 and Q_4; and the output buffer. The degenerated differential input pair shows highly linear behavior until

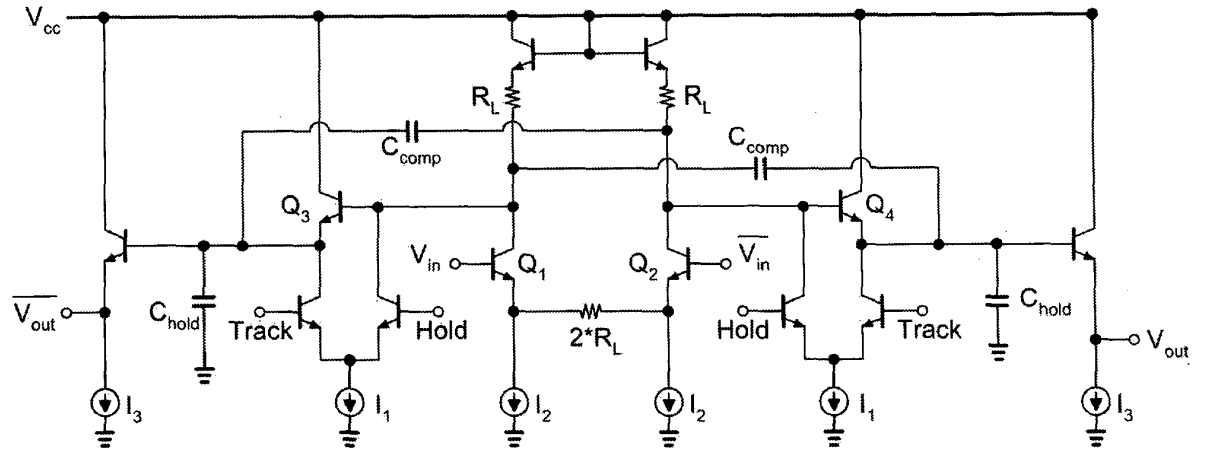

Fig. 2. Architecture of bipolar track-and-hold amplifier.

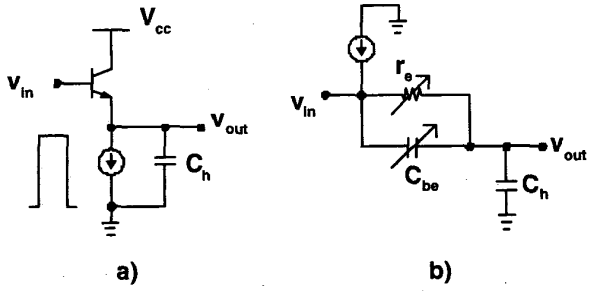

Fig. 3. (a) Switched emitter-follower sample-and-hold. (b) Small-signal equivalent circuit.

the tail current goes to zero in either of the input devices [4]. This occurs at an input voltage of $2I_2 * R_L$. For our circuit, the linear region extends to a peak input voltage of 2V, so the second stage, the SEF, bares the brunt of the linearity requirements.

Emitter-followers have inherent distortion mechanisms that must be overcome for a highly linear SHA and a Volterra analysis provides insight into the nonlinear behavior of the circuit(see Fig. 3). The nonlinear transfer function is given by:

$$v_{out} = H_1(j\omega_a)\cdot v_{in} + H_2(j\omega_a, j\omega_b)\cdot v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c)\cdot v_{in}^3 \quad (1)$$

The first order Volterra kernel below is identical to the behavior expected from the simplified model seen in Fig. 3. At low frequencies the SEF looks like a low pass filter; but at high frequencies it tends toward a capacitive divider. The size of the emitter-follower as well as the size of the hold capacitor determine the first-order transfer function of the SEF,

$$H_1(\omega_a) = \frac{1 + j\omega_a\tau_F}{1 + j\omega_a(\tau_F + r_e C_{hold})} \quad (2)$$

where τ_F is the forward transit time, C_{hold} is the hold capacitor, r_e is the base resistance, and ω_a is the frequency of the input signal. The second and third order Volterra kernels are found to be the following:

$$H_2(\omega_a, \omega_b) = \frac{[1 - H_1(j\omega_a)]^2(\frac{1}{2} + j\omega_a\tau_F)}{V_t[1 + j(\omega_a + \omega_b)(\tau_F + r_e C_{hold})]} \quad (3)$$

$$H_3 = \frac{(1 - H_1)^3(\frac{1}{6} + \frac{j\omega_a\tau_F}{2}) - (1 - H_1)H_2V_t[1 + j(\omega')\tau_F]}{V_t^2(1 + j(\omega_a + \omega_b + \omega_c)(\tau_F + r_e C_{hold}))} \quad (4)$$

where $\omega' = \omega_a + \omega_b$ and $V_t = kT/q$. And the third order intermodulation distortion is:

$$IM_3 = \frac{3}{4}\frac{|H_3(\omega_a, \omega_b, \omega_c)|}{|H_1(\omega_a)|^3} \cdot v_{in}^2 \quad (5)$$

(see Fig. 4). To confirm our new understanding, we can compare the response of the Volterra equations to that of a more simplified model. In this case, the emitter-follower driving a load capacitor. The 1dB compression point is simply $P_{1dB} = I_c/j\omega_a C_{hold}$. This can also be confirmed by looking at the third order distortion using Volterra analysis as a function of current. It can be shown that under normal circumstances, the 1dB compression point occurs approximately 10dB before the third order intercept point. A plot of the third order intercept point computed from the above Volterra analysis with the first order compression point as a function of bias current can be seen in Fig. 5.

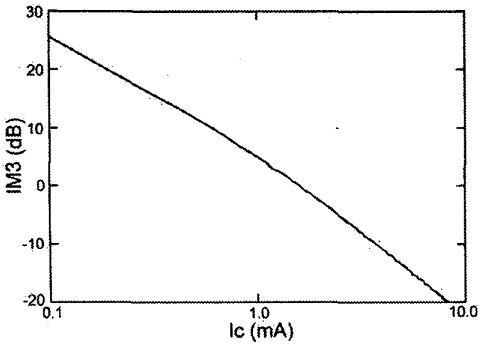

Fig. 4. IM3 - Third order intermodulation product calculated from Volterra analysis for a 1V input signal.

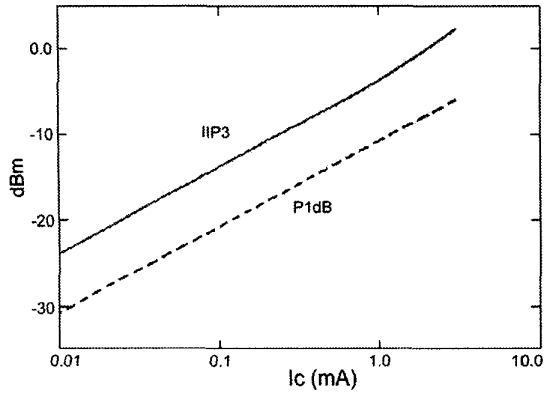

Fig. 5. Simulated P_{1dB} and IP_3.

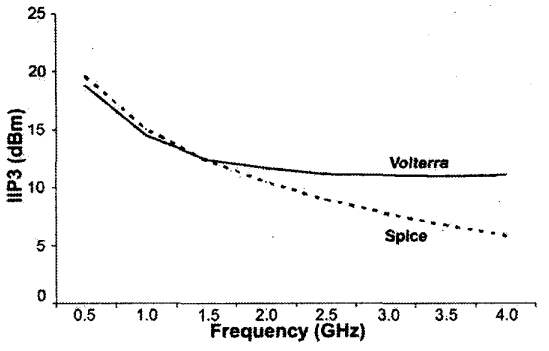

Fig. 6. Comparison of third-order intercept point. SPICE simulations and Volterra analysis ($C_{hold} = 500fF$, $I = 6mA$, and $\tau_F \approx 3.1ps$).

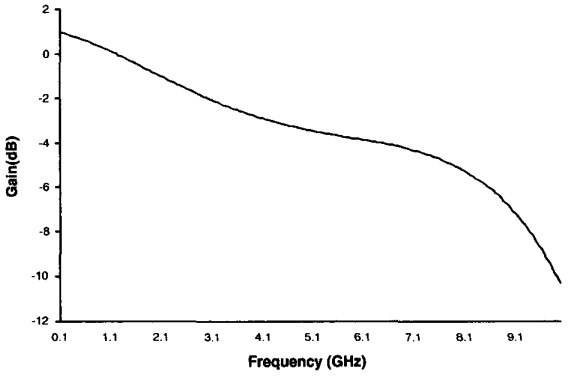

Fig. 7. Measured transfer function of track and hold amplifier in the track mode.

Simple SPICE model simulations also confirm our results. An emitter-follower was simulated driving a capacitive load and the third order intercept point was computed as a function of frequency. This is compared against the Volterra analysis and with similar results (see Fig. 6). The Volterra analysis guided selection of appropriate values for the bias current and the hold capacitor, C_{hold}, to yield a suitable IM3 performance.

III. Experimental Results

The sample-and-hold was fabricated in $0.5\mu m$ SiGe/Ge BiCMOS process with an active area of $0.150mm^2$ consuming 360mW in the THA core (see Fig. 10). It was designed to exist on die with a state-of-the-art ADC.

The performance was confirmed by several performance criteria. First, a single stage of the sample-and-hold was tested in track mode, to determine the track-mode distortion. Then, the sample-and-hold was tested in sub-sampling configuration to determine sampling distortion. Normally the SHA would be followed by an ADC that would be clocked at a short time before SHA transitions. The distortion is then measured at discrete moments in time. For our experiment, the continuous SHA output is sub-sampled and feed into a spectrum analyzer. In this manner the input and clock signals are tested at full speed. Thus, the full spectrum is analyzed, not just the held waveform normally presented to an ADC. In this manner, much more high frequency distortion is present at the output.

The clock signals were buffered on chip. The output signals were also buffered to 100ohms differential. Fig. 7 shows the transfer function of the THA in track mode. Difficulties in matching as well as excessive ripple from the high frequency off-chip baluns used in testing contributed to the ripple seen in the transfer function.

Two-tone intermodulation test was performed first in the track-mode alone and then in the full sampling mode. The third order intercept was computed to be greater than 26dBm with a dynamic range of greater than 46.2dB for almost all frequencies

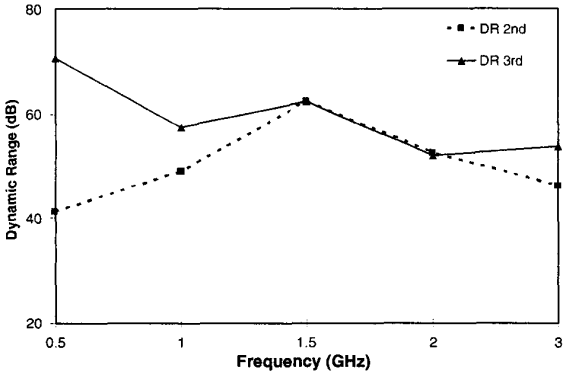

Fig. 8. Dynamic range of fundamental and second and third order products during the track-mode.

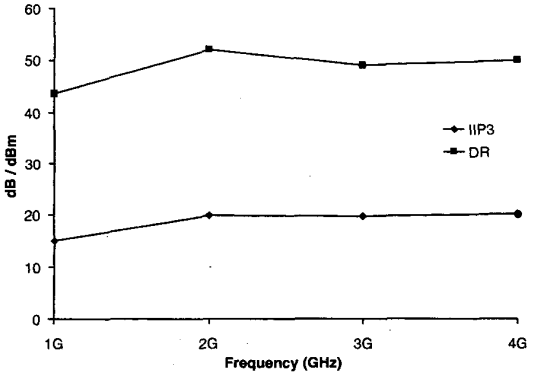

Fig. 9. IP_3 and dynamic range in sample-and-hold mode.

(see Fig. 8)

In full sampling mode, the dynamic range was greater than 43.5dB for up to 4GHz clock speed (see Fig.9).

IV. Conclusions

An improved design has been presented for a sample-and-hold circuit achieving wider bandwidth and lower distortion than previous circuits implemented in silicon technology (see Fig. I. An optimized switched-emitter follower design was used to extend the performance to higher frequencies. The aspects of the sample-and-hold design that lead to distortion at high frequencies were analyzed, and improvements in the circuit implemented to minimized these effects. The circuit exhibited an track-mode bandwidth of 6GHz and 8bit dynamic range. This circuit can be used as a building-block for next generation wide bandwidth communication systems.

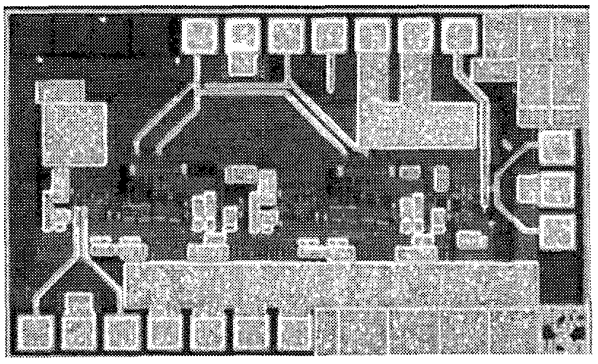

Fig. 10. Die photo.

TABLE I

Overview of High-Speed THAs

ref #	*Process*	*Res.*	*Fs*	*Fin*	*Power*
this work	SiGe HBT	8b	3.0GS/s	1.5GHz	0.72W
[3]	Si-HBT	8b	2.0GS/s	900MHz	0.55W
[5]	CMOS	8b	1.3GS/s	650MHz	
[6]	CMOS	6b	1.6GS/s	300MHz	
[7]	Si-Bipolar	8b	1.0GS/s	500MHz	0.44W
[8]	Si-Bipolar	10b	1.0GS/s	500MHz	0.164W
[9]	Si-Bipolar	10b	1.0GS/s	500MHz	0.30W

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