10.1 Digital-IF WCDMA Handset Transmitter IC in 0.25μm SiGe BiCMOS

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The wireless industry has evolved to enable high bit-rate communications, and the WCDMA system has emerged as a 3G standard. There is enormous pressure to reduce the size, cost, and power consumption of the mobile phone. While digital circuits have experienced tremendous power saving with the progress of deep sub-micron processes, the analog/RF sections remain the bottleneck in reducing the dc power consumption. This work focuses on the implementation of a highly integrated, low-power WCDMA transmitter IC (TxIC) that addresses this problem, through a combination of architecture and circuit innovations.

The heterodyne architecture is found in most existing WCDMA handset transmitters [1-2]; it is insensitive to leakage and dc offset issues, and is particularly well-suited to the wide output power range required of over 76 dB. Unfortunately, it also exhibits a high dc power dissipation and requires off-chip IF filtering. The homodyne architecture, while simpler and lower cost, suffers from degraded performance at low output powers, LO pulling, and a variety of other limitations. Our proposed approach features a digital IF modulator, as shown in Fig. 10.1.1 [3]. As the digital boundary is moved closer to the antenna, this architecture will take full advantage of silicon technology scaling. Furthermore, since modulation is performed digitally, near-ideal I/Q matching and enhanced error vector magnitude will result. Despite these well-known advantages, digital-IF approaches usually exhibit high power dissipation. Here, several innovations were derived to yield a simple, highly-integrated (with no off-chip IF filter), low-power solution. "Smart" dynamic biasing approaches were extensively employed, so the current consumption continuously adjusts to respond to the output power needs of the transmitter.

To simplify the IF filter design, we propose two solutions. First, the IF is selected so the DAC images appear out of the WCDMA Rx and Tx bands. This is satisfied if the clock rate is between 250 to 260MHz, and a value of 253.4MHz is selected. For the digital quadrature modulator, we impose the condition: $f_{IF} = f_{clk}/4$. As a result, the quadrature LO's will only take on values of +1, 0 or -1, and multiplication is a simple sign-bit flipping/zeroing.

Second, we implement a DAC that reduces image generation in the first place, minimizing spurious outputs. Traditional zero-order-hold (ZOH) DAC's attenuate the images with a sin(x)/x response. If the DAC produces "ramp" outputs (or a "first-order-hold" (FOH) reconstruction), the images will roll off at the elevated rate of $(\sin(x)/x)^2$. The implementation of a FOH DAC is similar to a conventional current-steering DAC. A current is generated that is proportional to the difference between two consecutive input digital codes (digital differentiation), and then the current is delivered to a capacitor to perform the I-to-V conversion (analog integration). A K^{th}-order-hold DAC with $(\sin(x)/x)^{K+1}$ response is implemented by cascading K digital differentiators and K analog integrators. Simulations show that when a second-order-hold (SOH, K = 2) DAC is employed, the WCDMA spurious emission requirements are met with no dedicated reconstruction filter.

The 250MHz SOH DAC includes an 8-bit current-steering DAC with a dominantly capacitive load, and the IFVGA functions as second integrator. Figure 10.1.2 shows the DAC core. The capacitive load, together with the fast bipolar npn switches, allow high speed conversion at very low bias current – a key issue with digital-IF approaches. The common-mode output voltage is set by a pair of large resistors, which also damp the otherwise ideal integrator and prevent it from saturating.

To reduce the mirror ratio and therefore the power consumption, we employ a 16:1 capacitor current divider. It divides the current coming from the lower LSB segment (last 4 bits) by 16, and sums it with the upper segment (first 5 bits) current. The current ratio is reduced from 256:1 to 16:1, and the DAC power consumption is substantially reduced, consuming 8mA with a 3V supply. The measured DAC output spectrum (from dc to 1GHz) for a full-scale single-tone sine wave, at the output of the IFVGA, is shown in Fig. 10.1.3. It exhibits the elevated $(\sin(x)/x)^3$ roll-off, satisfying the WCDMA spurious requirements. A SQNR of 50dB is measured over the Nyquist band, confirming 8-bit resolution at the IF frequency. WCDMA adjacent channel power rejection (ACPR) is measured to be -44dB.

In the case of a relatively low IF of 63.4MHz, the variable gain single-sideband mixer is efficiently achieved with a translinear IF input stage, so the power consumption reduces from 30mA (high-gain) to 14mA (low-gain). The measured sideband rejection meets the specifications at -28dBc, while the LO leakage at maximum power level is -42dBc.

The RFVGA is a two-stage (cascode and common-emitter) design shown in Fig. 10.1.4. The key is to keep the quiescent current as low as possible, and allow the amplifier to achieve higher average current (Class AB) only when needed; "smart" adaptive bias schemes are employed. The common-emitter amplifier features a constant base voltage bias using an active buffer, while the cascode amplifier implements a power detector bias control. Designed for deep Class-B operation, the power detector control circuit produces a dc current (I_{ave}) proportional to the amplitude of the input signal. The extra current is mirrored (with a digitally controlled multiplying factor) and summed with the bias of the main cascode amplifier.

The measured RFVGA gain is 16dB at the quiescent current (I_{eq}) of 9mA. Due to the dynamic bias, gain compression is compensated by gain expansion, resulting in enhanced dynamic range without an increase in quiescent dc power. The output 1dB compression point is improved by 3.5dB to +12.7dBm. The RFVGA linearity is also improved as shown in Fig. 10.1.5. At the maximum average WCDMA power level of 3.5dBm, the detector circuit has improved the ACPR by 6dB. The ACPRs at 5MHz and 10MHz equal -43dB and -59dB, respectively.

Fabricated in IBM's 0.25μm SiGe BiCMOS process, the TxIC chip is shown in Fig. 10.1.7. The chip contains 6 inductors, 400 capacitors, 320 npn transistor's and measures 1.8 x 2.2mm^2. The TxIC current consumption, as well as some key measured results, are shown in Fig. 10.1.6. No clock spurs (except the clock leakage) will land in the Rx band. The relatively high noise at the Rx band is due to the unfiltered DAC quantization noise, which can be mitigated by adding extra poles to the IFVGA if necessary. The TxIC consumes 58mA at the maximum average output power of 3.5dBm, decreasing to 41mA at reduced gain.

References:

[1] A. Bellaouar et al., "A Highly-Integrated SiGe BiCMOS WCDMA Transmitter IC," *ISSCC Dig. Tech. Papers*, pp. 238-239, Feb. 2002.

[2] P. Chominski et al., "A Highly-Integrated Si/SiGe BiCMOS Upconverter RFIC for 3G WCDMA Handset Applications," *Proc. ESSCIRC,* pp. 447-450, Sept. 2002.

[3] V. Leung et al., "An Improved Digital-IF Transmitter Architecture for Highly-Integrated W-CDMA Mobile Terminals," *IEEE Vehicular Tech. Conf.*, vol. 2, pp. 1335 -1339, Apr. 2003.

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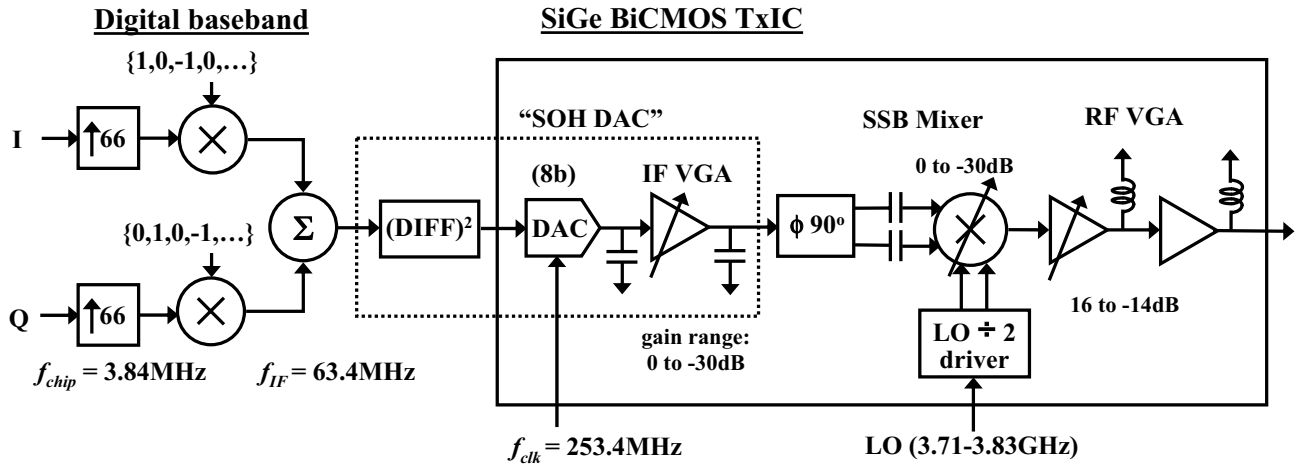

Figure 10.1.1: WCDMA digital-IF transmitter architecture.

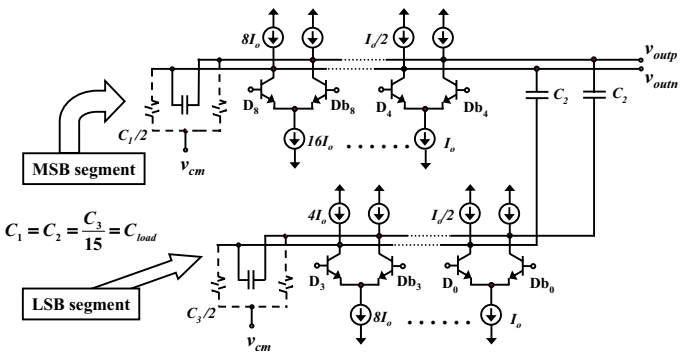

Figure 10.1.2: SOH current-steering DAC core.

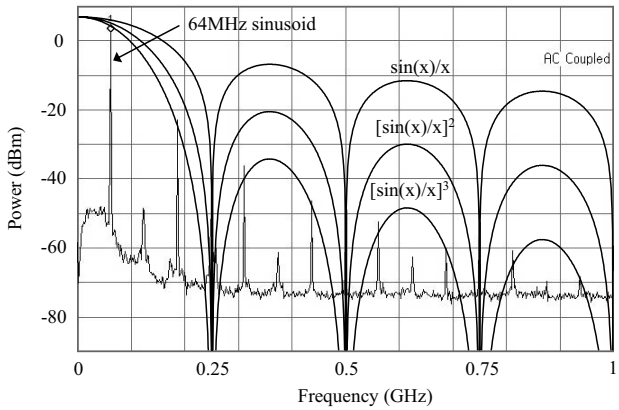

Figure 10.1.3: Measured SOH DAC output spectrum.

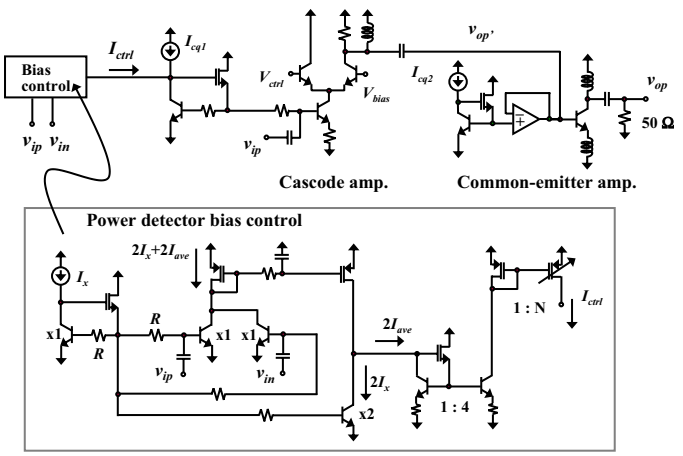

Figure 10.1.4: RFVGA with active bias control.

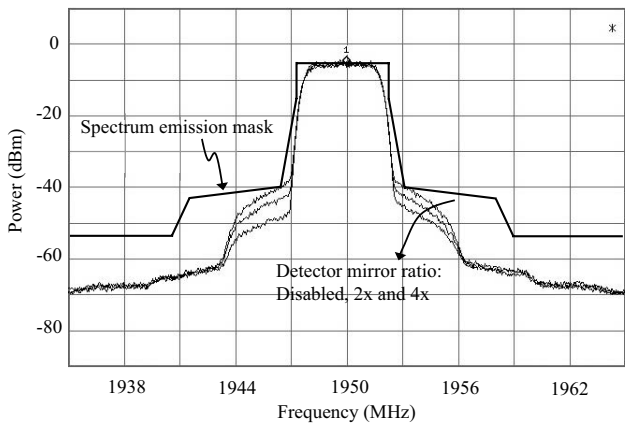

Figure 10.1.5: Measured ACPR of RFVGA. (Pout=3.5dBm)

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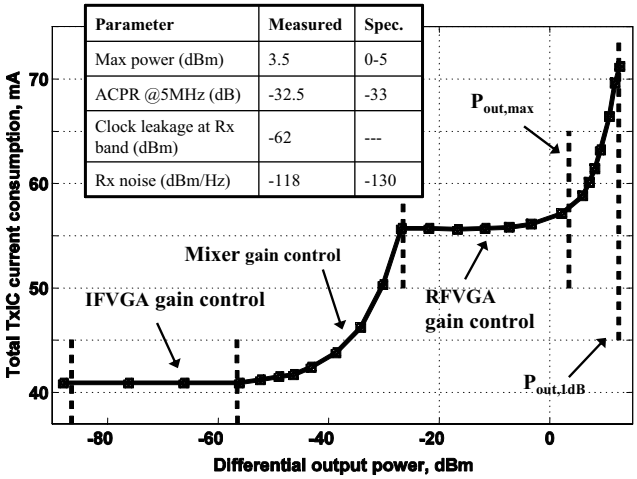

Figure 10.1.6: Summary of key TxIC performances.

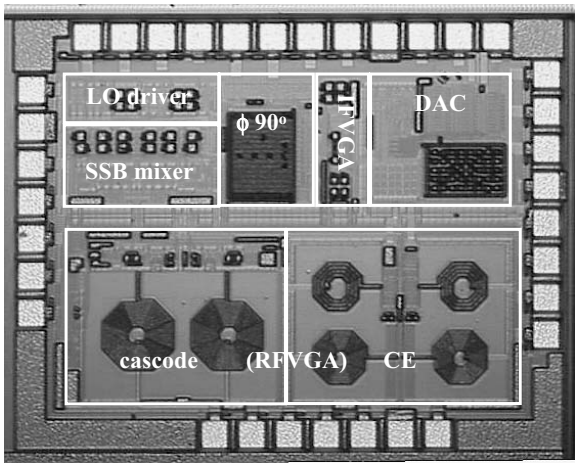

Figure 10.1.7: TxIC die photo.

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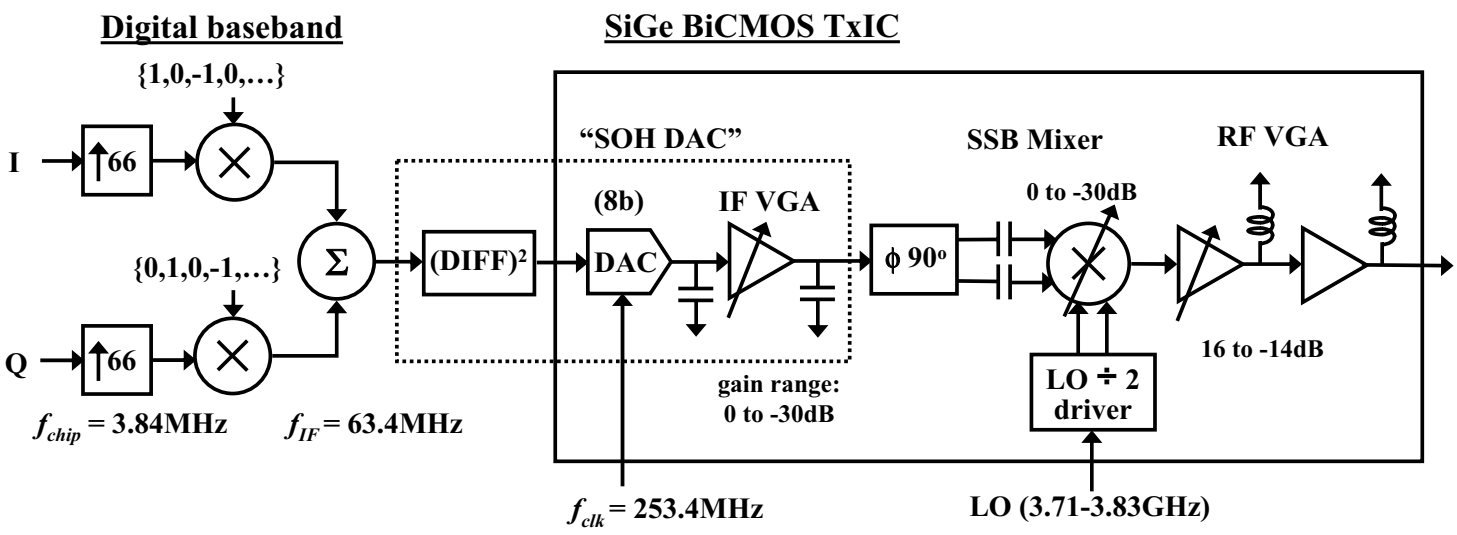

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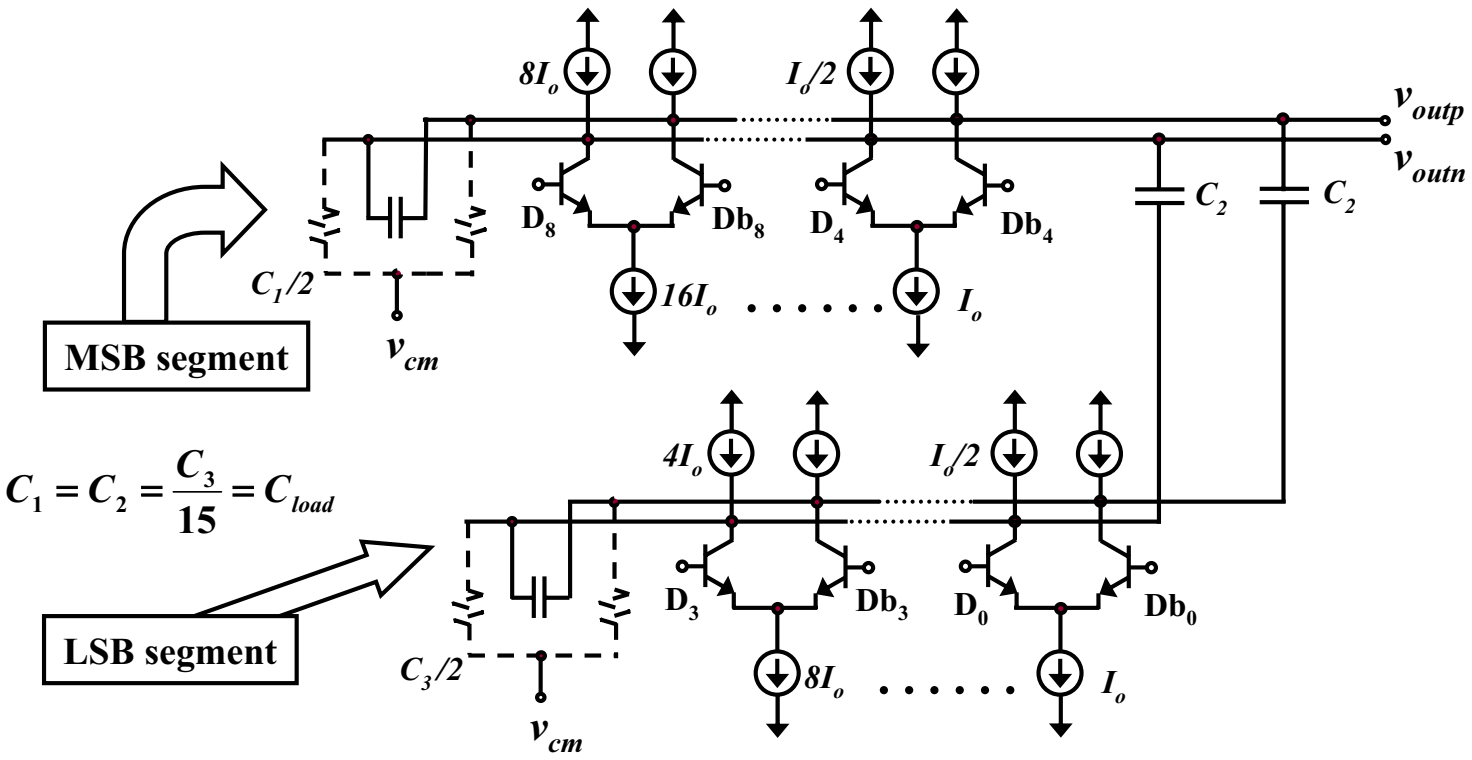

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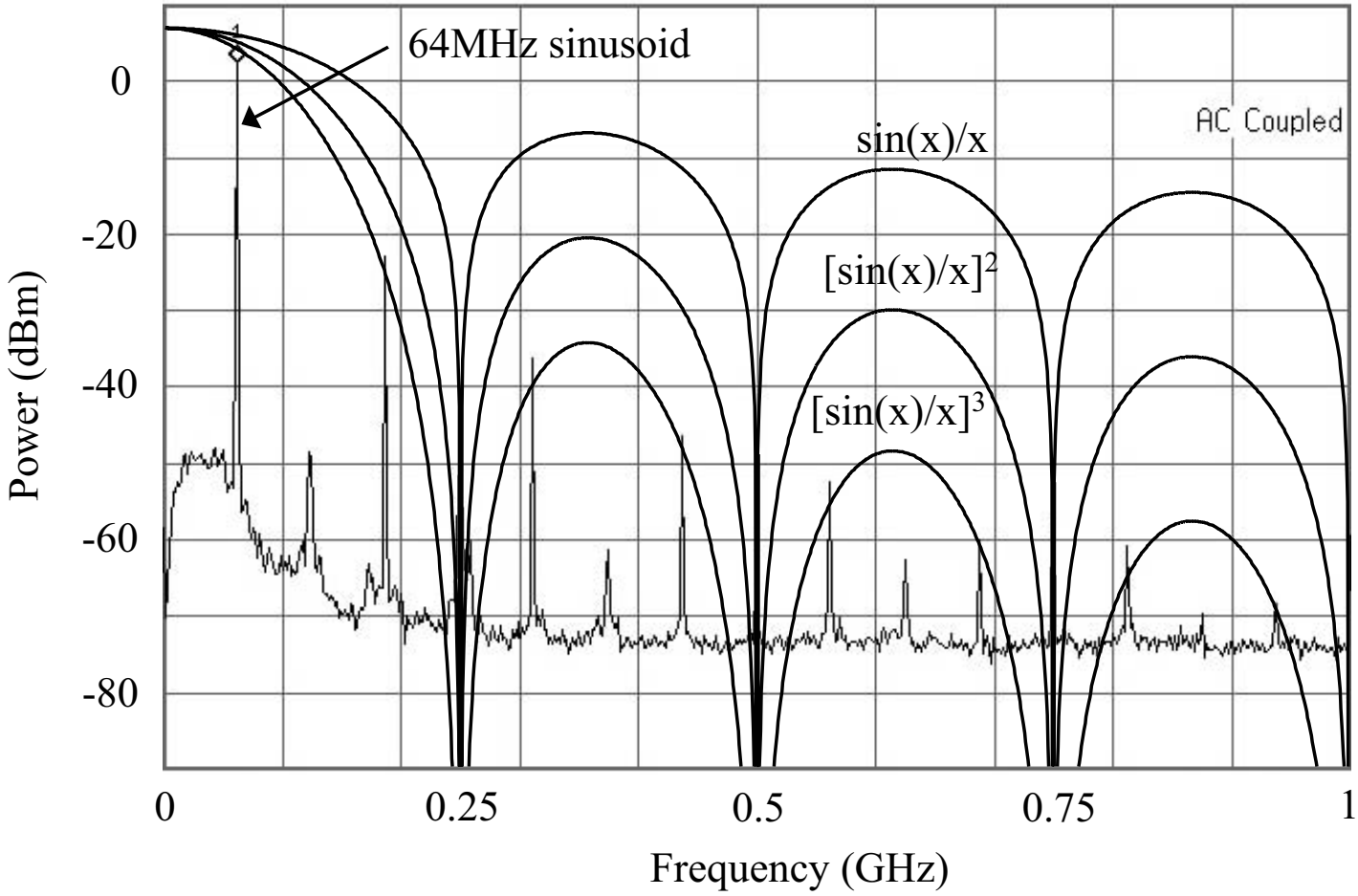

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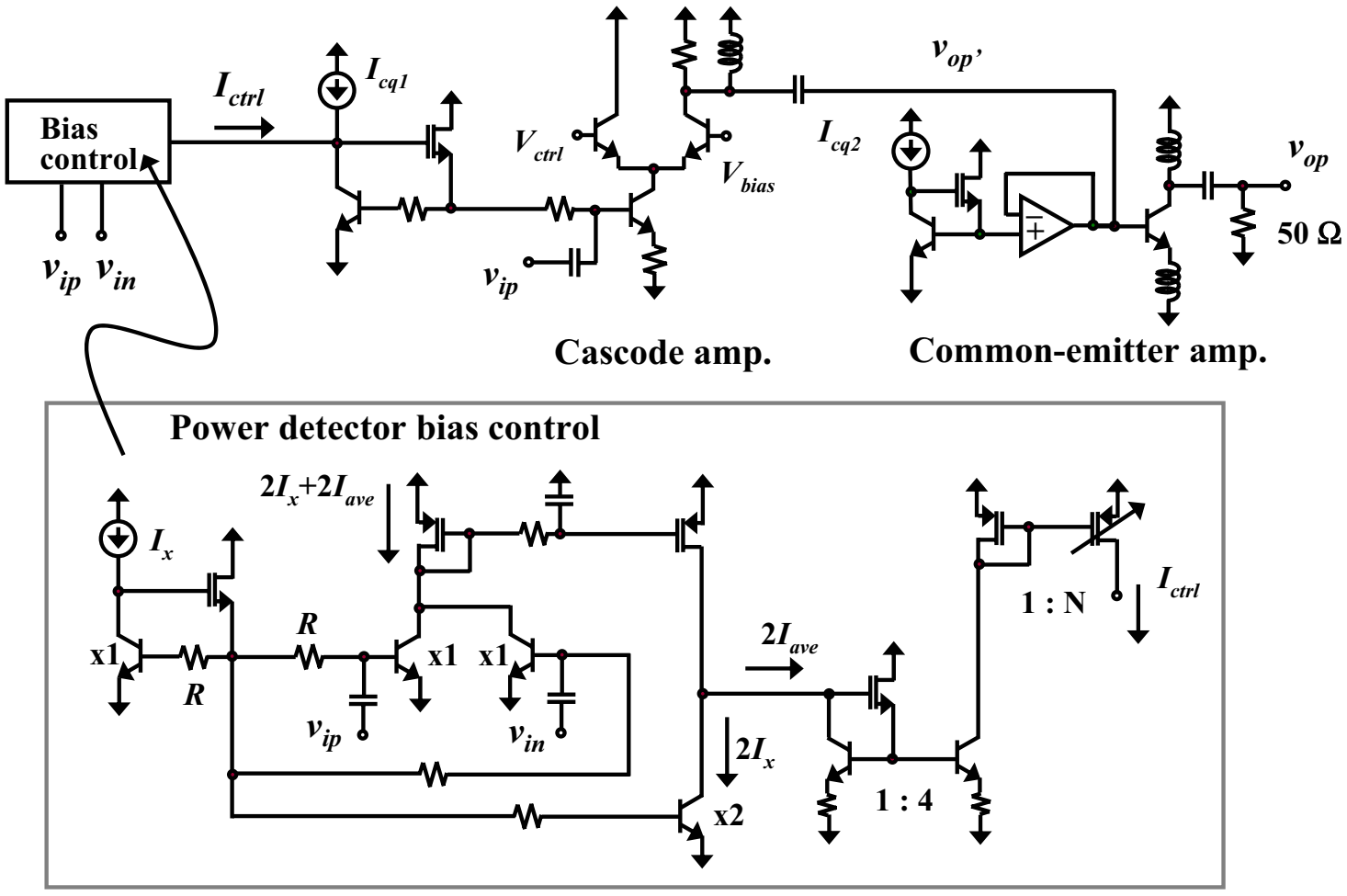

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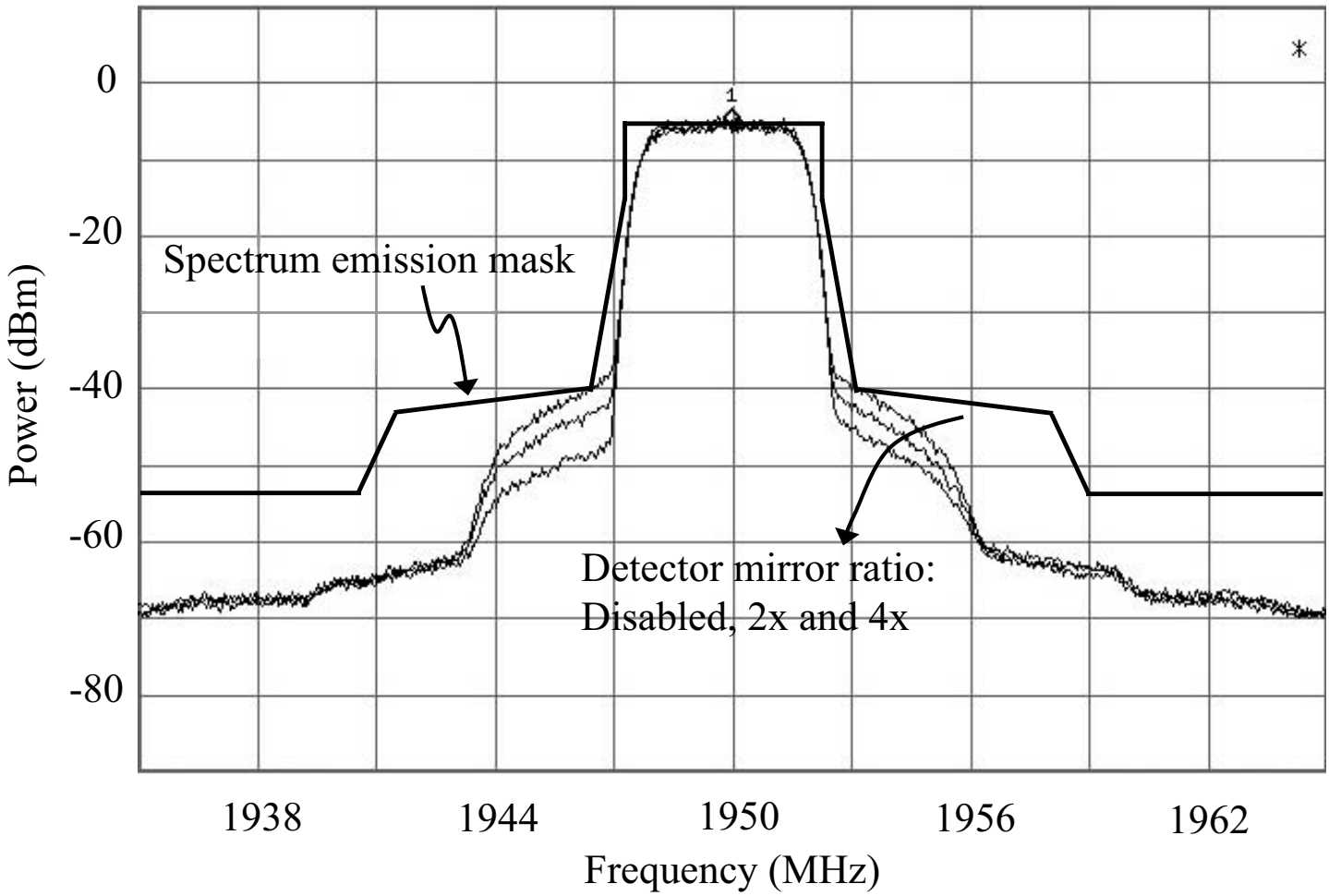

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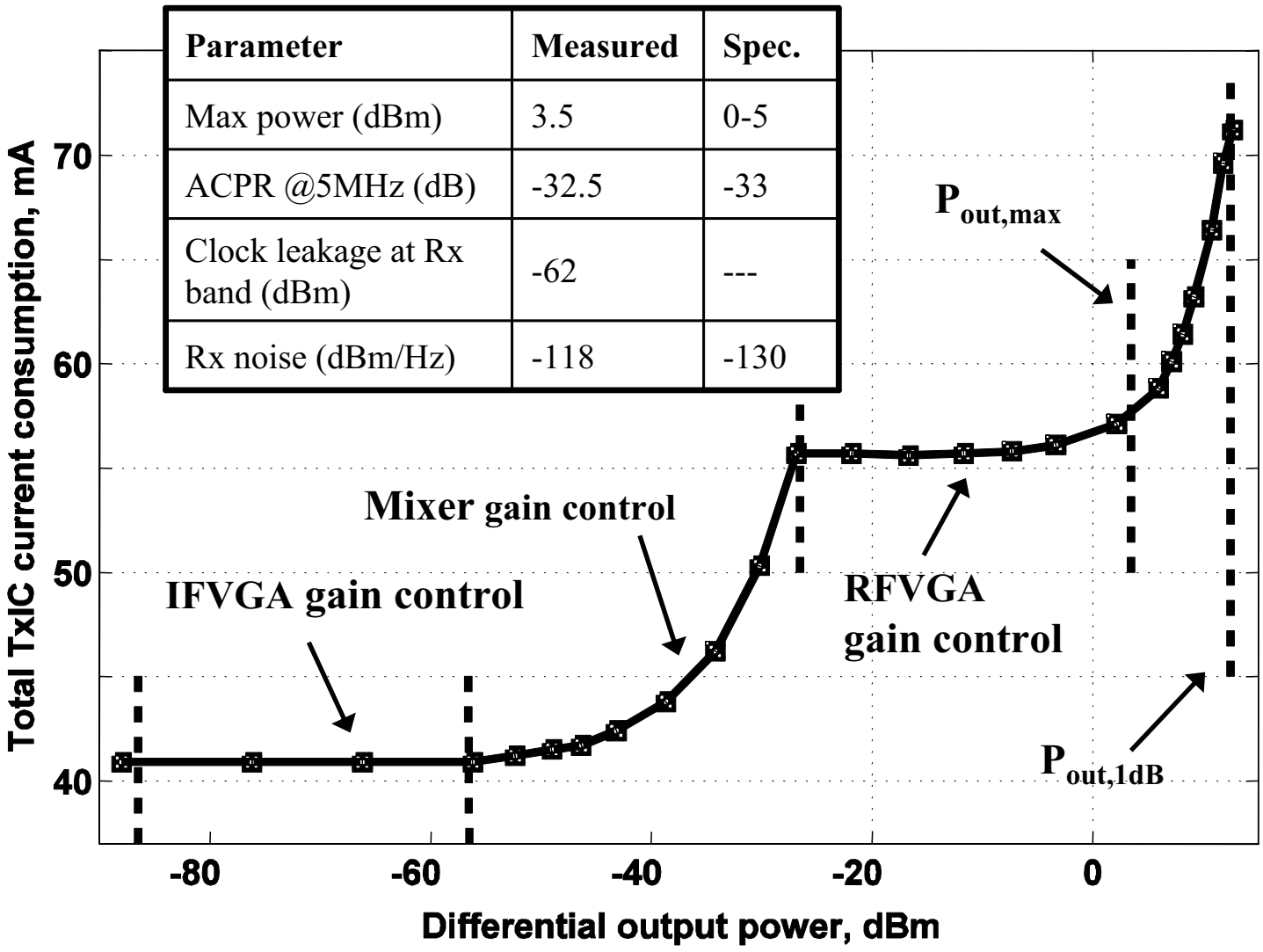

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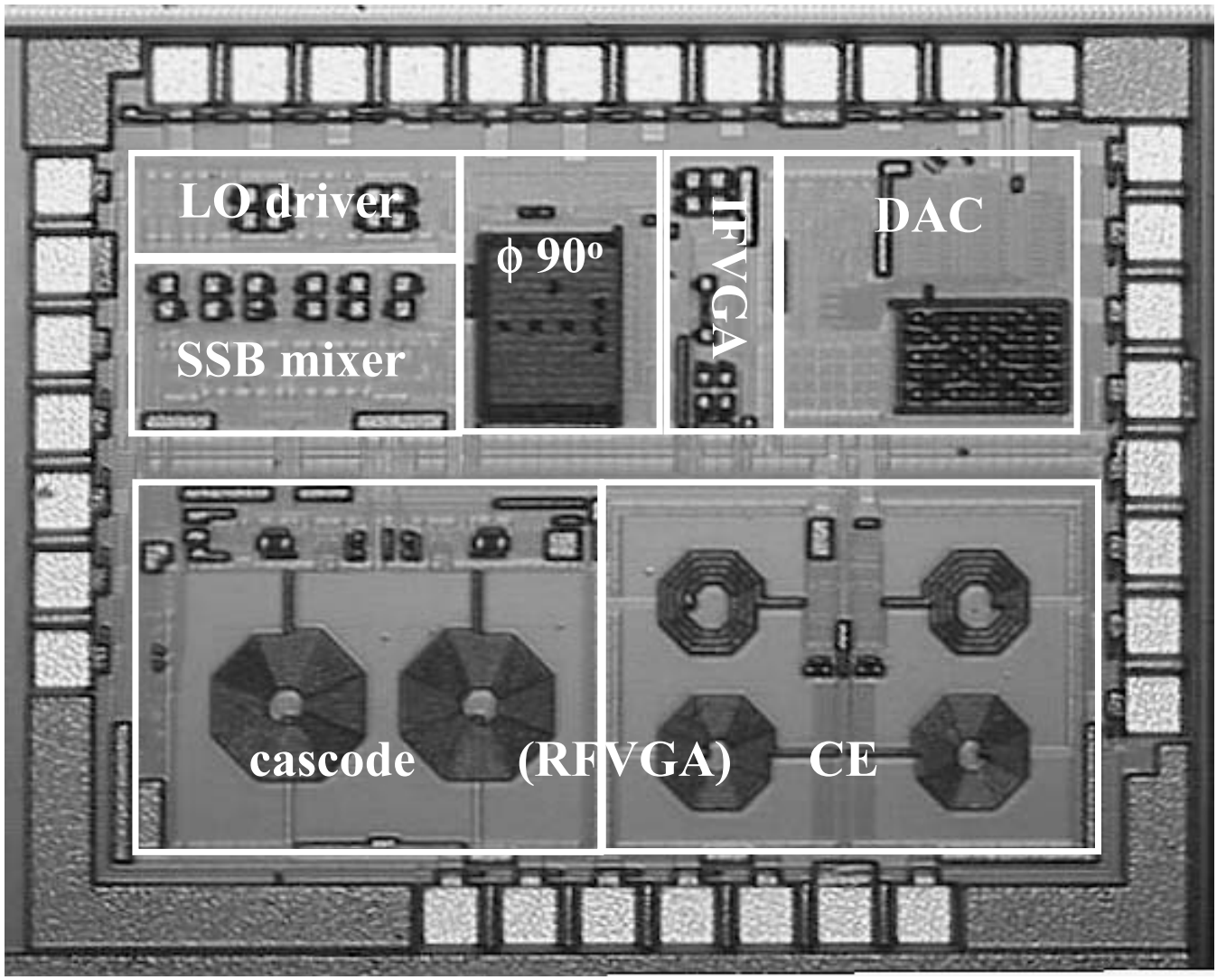

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