An Improved Digital-IF Transmitter Architecture for Highly-Integrated W-CDMA Mobile Terminals

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Abstract—**An improved digital-IF transmitter architecture for W-CDMA mobile terminals is proposed. Based on the heterodyne design but without requiring any off-chip IF filter, the transmitter enjoys the advantages of a homodyne architecture (such as circuit simplicity, low power consumption and high level of integration) while avoiding the performance problems associated with direct up-conversion. By implementing the quadrature modulation in the digital domain, and requiring only a single path of analog baseband circuits, inherently perfect I/Q matching and good EVM (error vector magnitude) performance can be achieved. The intermediate frequency (IF) is chosen to be a quarter of the clock rate for very simple and low-power digital modulator design. The difficulties of on-chip IF filtering were greatly alleviated by (a) performing a careful frequency planning, and (b) employing a special-purpose DAC to produce high-order sin(x)/x rolloff. System level simulation demonstrates that spurious-emission requirements are met with virtually no dedicated reconstruction filter circuits. This architecture takes full advantage of CMOS technology scaling by employing digital processing to ease analog complexities.**

Keywords—W-CDMA, mobile station, transmitter architecture, integrated circuit, digital IF, quadrature modulator, reconstruction filtering, frequency planning, high-order-hold DAC

I. INTRODUCTION

Virtually all existing commercially available W-CDMA handset transmitters are heterodyne [1,3-6], performing RF up-conversion in 2 steps as shown in Figure 1(a). This architecture offers many advantages, most importantly, the very wide gain control range of 76 dB demanded by the W-CDMA standard [7] can be distributed to two variable gain amplifiers (VGA's) in IF (intermediate frequency) and RF (radio frequency) bands. The resulting RF VGA that has a lowered gain range can then be efficiently designed within the limit imposed by the substrate isolation at high frequencies.

However, heterodyne architecture often demands external IF filters [1,4,5]. These off-chip components would substantially increase the size and cost of the chipset, and are therefore highly unappealing. Two approaches have been attempted to eliminate them. The design of [3] employs an active IF poly-phase filter, while the architecture of [6] adopts a meticulous frequency plan so that the copious spurs, even left un-attenuated, would not violate the spurious specifications.

The second drawback of the heterodyne architecture is that two synthesizers (IF and RF) are needed [1,4,5], which lead to relatively complicated and power hungry designs. The designs of [3] and [6] mitigate this problem by employing a "variable IF" scheme, where both up-conversion mixers are driven by a common synthesizer.

On the other hand, if the baseband I/Q signals are up-converted to the RF directly, the above problems (namely the external SAW filter and multiple synthesizers) could be avoided. The design of [2] features this so-called homodyne architecture as shown in Figure 1(b). Obviously, it demands no IF filtering, and it requires only one synthesizer.

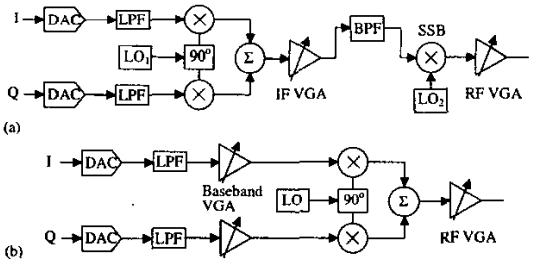

Figure 1. Block diagrams of (a) the heterodyne, and (b) the homodyne transmitter architecture

However, the homodyne suffers serious performance issues not seen in its heterodyne counterpart. Notice that due to limited substrate isolation at high frequencies, most of the gain control must now be implemented at the baseband (dc) section, leading to limited dynamic range. A small LO leakage (which lies in the transmit channel), or a low gain/phase mismatch between the baseband VGA's (or the quadrature mixers), can lead to severe degradation of error vector magnitude (EVM). We believe that the homodyne approach is in fact more problematic than it first appears.

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In this work, we propose an improved heterodyne transmitter IC (TxIC) architecture that leverages the rapid technology advancement in CMOS by implementing the IF up-conversion digitally. By means of a simple digital quadrature modulator, a careful frequency planning, and a second-order-hold D/A converter, our architecture (a) eliminates the external IF filter, (b) demands only one synthesizer, (c) employs only one RF (analog) quadrature mixer, and (d) achieves inherently perfect I/Q matching (for good EVM performance). In short, our TxIC inherits the advantages of the homodyne architecture without suffering the accompanying performance degradations.

II. TRANSMITTER ARCHITECTURE

A. *Transmitter Architecture Overview*

Figure 2 shows the proposed architecture, which is a digital IF heterodyne transmitter. Digital data (at 3.84MHz chip rate) are up-sampled (interpolated), filtered, multiplied with the quadrature LO's, and then summed together before they reach the digital-to-analog converter (DAC). As such, the DAC should be designed to handle the (much faster) IF signal, although only one DAC is needed (instead of two, see Figure 1(a)).

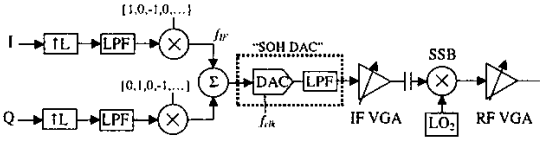

Figure 2. Heterodyne transmitter with digital IF modulator

Since the quadrature up-conversion is performed digitally and there is no separate I and Q analog path, perfect I/Q matching and EVM performance can be achieved [8][1]. In addition, ac coupling is possible because the analog signal is no longer centered at dc. As a result, the dc offset of the analog circuits before the single sideband (SSB) mixer is eliminated, and consequently, will not cause LO leakage.

To fully realize the potential of our architecture for the W-CDMA handset applications, and achieve our objectives stated earlier, we are proposing several innovative design ideas, which will be discussed next.

B. *Digital Quadrature Modulator*

In general, the digital modulator demands numerical oscillators and multipliers, resulting in complicated and power-hungry design. However, it can be significantly simplified if we impose:

$$f_{IF} = f_{clk}/4 \qquad (1)$$

That is, if the intermediate frequency (f_{IF}) is to be a quarter of the DAC clock rate (f_{clk}), the LO signals can be completely represented by values of +1, 0 or -1. Therefore, the digital modulator is but a trivial sign-bit-flipping logic[2], thus eliminating the need for a direct digital synthesis (DDS) or a general digital multiplier. This lowers the power budget of the modulator considerably.

Under this scheme, we do not have freedom to choose the frequency (or the phase) of the LO signals once the DAC clock rate is determined. However, for the mobile phone applications, this is not an issue at all. This is because only one channel is transmitted per station at a time, and the RF mixer with its VCO (i.e. LO_2 of Figure 2) will subsequently up-convert the IF signal to any desired channel frequency.

C. *Problem of Reconstrustion (IF) Filtering*

In a digital-to-analog conversion system, repeating IF spectra would appear around the multiples of the clock frequency. These "digital images" would occupy frequencies of $f_{clk} \pm f_{IF}$, $2f_{clk} \pm f_{IF}$, and $3f_{clk} \pm f_{IF}$, etc.). To prevent them from interfering with other sensitive frequency bands, and to meet the spurious emissions requirements, lowpass (reconstruction) filtering is required following the DAC.

Although the condition imposed in (1) allows easy digital modulator design, the reconstruction filtering can become difficult due to the low oversampling ratio (OSR $= (f_{clk}/2)/f_{IF} = 2$). The DAC digital images will show up very close in frequency to the desired signal. If they are to be sufficiently attenuated on-chip, high-order linear-phase automatically-tuned filter is necessary. To appreciate this problem in our W-CDMA mobile phone environment, where the transmit (Tx) band is between 1920 to 1980 MHz and the receive (Rx) band 2110 to 2170 MHz, let's consider two scenarios. The discussion will subsequently lead us to choosing an optimal IF (thus the DAC clock speed and the interpolation factor L) for easy reconstruction filter design.

a) Case 1: If an interpolation factor of 16 (L=16) is chosen, the DAC clock will be running at $3.84 \times 16 = 61.44$ MHz, giving an IF of 15.36 MHz. For a Tx channel located at, say, 1940 MHz, the first image will also appear in the Tx band. This is shown in Figure 3 (a). To ensure 55 dB of image attenuation at Tx band, and a level of phase linearity commensurating -42 dB EVM, a 5th-order Butterworth lowpass filter with a 18 MHz cutoff frequency is demanded. While such a design is not technically prohibitive, it is certainly non-trivial and should be avoided if possible.

b) Case 2: If the interpolation factor is chosen to be 32, the DAC clock will be running at 122.88 MHz, and the intermediate frequency is 30.72 MHz. The Tx spectrum is shown in Figure 3 (b). Here, although no image falls into the

[1] In the single-sideband (SSB) mixer, a 90° phase shifter will act on the single analog input and generate two quadrature signals. The inevitable I/Q mismatches of the circuit would result in a residual (imperfectly rejected) sideband. It would not, however, impact the EVM performance of the desired transmit channel.

[2] In fact, the quadrature LO signals can be equivalently represented by sequences of {+1,+1,-1,-1,+1,+1,...} and {-1,+1,+1,-1,-1,+1,...}. Therefore, multiplication is simply accomplished by inverting the sign bits of every two consecutive input baseband data.

Tx band, the image in the Rx band still needs to be sufficiently filtered. To achieve 61dB of attenuation with -42dB of EVM performance, a 4th-order Butterworth lowpass filter with 40 MHz cutoff frequency is required. Despite its lower order, this filter design is no simpler because of the higher cutoff frequency.

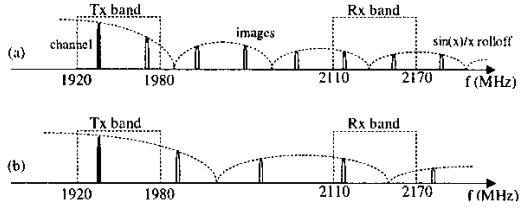

Figure 3. Locations of digital images when (a) L=16, and (b) L=32.

As demonstrated above, this brute force filtering effort could be difficult and power hungry. However, the problem can be greatly alleviated by (a) performing optimized frequency planning, and (b) employing a high-order-hold DAC. Both will be discussed below.

D. Frequency Planning Scheme

If the clock frequency is strategically selected so that the DAC images will appear out of the frequency bands of interest, the filter requirement could be substantially relaxed. Our goal is to make sure that no DAC images will land into the sensitive Transmit (Tx, 1920-1980 MHz) and Receive (Rx, 2110-2170 MHz) bands for all transmit channel locations. This can be met if the Rx band is always between the 1st and the 2nd images for all channel locations, as shown in Figure 4. Notice that after RF up-conversion, the 1st and the 2nd images are given by,

$$\begin{aligned} f_{imag1} &= f_{ch} + f_{clk}/2 \\ f_{imag2} &= f_{ch} + f_{clk} \end{aligned} \tag{2}$$

where f_{ch} denotes the channel location, which is between 1920 to 1980 MHz (Tx band). To ensure that the 1st image is always below the lower edge of the Rx band, we can write

$$\begin{aligned} f_{ch} + f_{clk}/2 &< 2110 \\ f_{clk} &< (2110-1980)\times 2 \\ f_{clk} &< 260 \text{ (MHz)} \end{aligned} \tag{3}$$

Similarly, to ensure that the 2nd image is always above the upper edge of the Rx band, we can write

$$\begin{aligned} f_{ch} + f_{clk} &> 2170 \\ f_{clk} &> 2170-1920 \\ f_{clk} &> 250 \text{ (MHz)} \end{aligned} \tag{4}$$

Combining the results found in (3) and (4), we arrive at

$$250 < f_{clk} < 260 \text{ MHz} \tag{5}$$

In summary, if the clock rate is set to be between 250 to 260 MHz, no digital images will land into the Tx or the Rx bands. This can be achieved by choosing an integer up-sampling ratio (L) of 66. The DAC clock and the IF frequencies are 253.4 and 63.4 MHz, respectively. A second-order filter will be sufficient to reject the digital images and meet the spurious emission requirements.

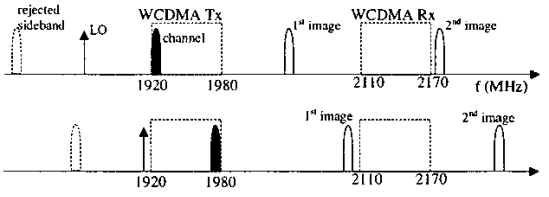

Figure 4. Frequency planning illustration: locations of images when the channel is at the lower or the upper edge of the Tx band.

This relaxed filter requirement is achieved at the expense of a high clock rate— the last stage of the baseband digital logics, as well as the DAC, are running in the excess of 250 MHz. The dynamic (digital) power consumption can be high. However, with the advancement of fine-geometry processes, the dynamic power consumption is being driven down very rapidly. Therefore, we believe it is a reasonable technology direction to trade off analog filter complexity with faster digital clock speed.

E. High-Order-Hold DAC

As the second part of our solution to address the reconstruction filter problem, we derived a DAC which "avoids" generating images in the first place.

A conventional DAC produces the analog waveform by converting the digital "sample" into an analog voltage, and "holding" it for one clock period until the next sampling instance. Such a sample-and-hold (S/H) waveform will exhibit repeating digital spectrum with the familiar $\sin(x)/x$ (sinc) rolloff, as shown in Figure 5(a). This is also known as zero-order-hold (ZOH) in the signal processing literature.

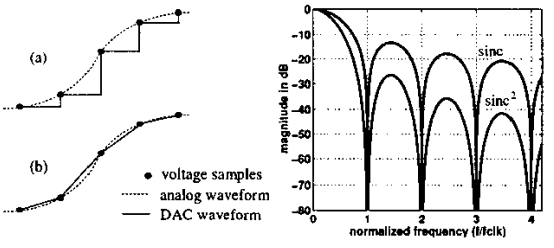

Figure 5. Transient waveforms of (a) S/H DAC and (b) FOH DAC, and their corresponding spectrum rolloffs.

The energy of images can be greatly reduced if the DAC output waveform is less abrupt than the staircase shown above. Instead of performing an S/H, the DAC could connect the voltage samples by straight lines like a ramp as shown in Figure 5(b). It performs what is commonly known as "first-order-hold" (FOH) reconstruction, and exhibits $(\sin(x)/x)^2$ (sinc squared) spectrum where images roll off much faster.

The circuit implementation of the FOH DAC is very straightforward. First, a current is generated which is proportional to the *difference* between 2 consecutive input digital codes (digital differentiation). Second, the current is pumped into a *capacitor* to perform the I-to-V conversion (analog integration). As such, the capacitor voltage will ramp up, effectively connecting one analog sample to the next. The implementation of a FOH DAC is in fact very comparable to that of a standard S/H (current-steering) DAC, as demonstrated in Table I.

TABLE I. COMPARSION BETWEEN THE CONVENTIONAL S/H DAC AND THE FOH DAC

	S/H DAC	FOH DAC
current (I) generation	Proportional to the input digital codes	Proportional to the *difference* between 2 input consecutive digital codes
Load	Resistor (R)	Capacitor (C)
Voltage output (V)	$V = I \cdot R$	$V = \frac{1}{C}\int (I)dt$
Waveform	Zero-order-hold	First-order-hold
Spectrum	$\sin(x)/x$ rolloff	$(\sin(x)/x)^2$ rolloff

Based on our intuitive understanding of the FOH DAC circuit implementation, we can represent its signal processing in Figure 6(a), in which a digital differentiator $(1-z^{-1})$ is followed by an analog integrator[3], $(1/T)\int dt$ (where T is the clock period). Essentially, the cascade of the digital differentiator and the analog integrator will turn the ZOH (square) pulse of $h_0(t)$ into a FOH (triangular) pulse of $h_1(t)$. The Laplace transform of a square pulse $h_0(t)$ [9] is given by

$$H_0(\omega) = T \cdot \left[\frac{\sin(\omega T/2)}{\omega T/2}\right] \cdot e^{-j(\omega T/2)} \tag{6}$$

where T is the sample (clock) period. Referring to Figure 6(a), the Laplace transform of the triangular pulse $h_1(t)$ can be written as

$$\begin{aligned} H_1(\omega) &= (1-e^{-j\omega T}) \cdot \frac{1}{j\omega T} \cdot H_0(\omega) \\ &= T \cdot [\frac{\sin(\omega T/2)}{\omega T/2}]^2 \cdot e^{-j\omega T} \end{aligned} \tag{7}$$

As shown in (7), the final FOH DAC waveform will exhibit a spectrum with $(\sin(x)/x)^2$ rolloff.

[3] The FOH DAC signal processing suffers a "singularity" at dc. Infinite attenuation of the differentiator is met by the infinite amplification of the integrator. However, this poses no problem to our application because the (IF) signal is bandpass in nature. We only need to avoid dc offset from saturating the integrator by performing a damped integration or a simple ac coupling.

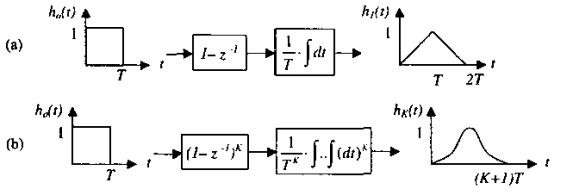

Figure 6. Signal processing of (a) a FOH DAC and (b) a K[th]-order hold DAC.

The previous ZOH to FOH transformation can be generalized to realize any high-order-hold DAC. If we cascade K digital differentiators with K analog integrators as shown in Figure 6(b), we can turn a ZOH pulse into a K[th]-order-hold pulse,

$$\begin{aligned} H_K(\omega) &= (1-e^{-j\omega T})^K \cdot \frac{1}{T^K} \cdot \frac{1}{(j\omega)^K} \cdot H_0(\omega) \\ &= T \cdot [\frac{\sin(\omega T/2)}{\omega T/2}]^{K+1} \cdot e^{-j(K+1)\omega T/2} \end{aligned} \tag{8}$$

Therefore, the K[th]-order-hold DAC will exhibit $(\sin(x)/x)^{K+1}$ rolloff. To the extreme, when K is high, the digital images will be so small in the DAC output spectrum, and the DAC time-domain waveform will resemble the "true" (very smooth) analog signal very well.

Figure 7 illustrates how the output waveforms look like for the ZOH, the FOH, and the second-order-hold (SOH, K=2) DAC's. Notice that the three DAC's produce the same voltages at the sampling instances (after proper time alignment as they have different phase shifts). It is obvious that the higher the order, the smoother the DAC waveform.

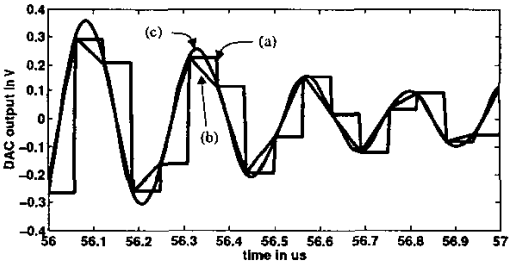

Figure 7. Output waveforms of the (a) ZOH, (b) FOH, and (c) SOH DAC

F. *Summary of the Transmitter Architecture*

Figure 8 shows the block diagram of the final transmitter architecture with all the design parameters as described earlier. The SOH DAC is selected to provide a $(\sin(x)/x)^3$ spectrum for high image rolloff [4]. It is composed of two digital

[4] An inverse $(\sin(x)/x)^3$ digital filter (not shown in Figure 8) is needed to compensate for the in-channel distortion of the baseband signals. While more complicated than a conventional inverse $(\sin(x)/x)$ filter, it should not be too

differentiators and two continuous-time integrators in cascade. The first continuous-time integrator is built as a FOH DAC, while the second one is naturally incorporated into the IF VGA outputs. No dedicated reconstruction filter circuit, or precision automatic tuning, is needed. This scheme can be understood as performing digital pre-emphasis on the baseband signals to trivialize the task of analog filtering. Again, this follows the same technology direction discussed earlier. That is, to trade off analog complexities by implementing more functions in the digital domain.

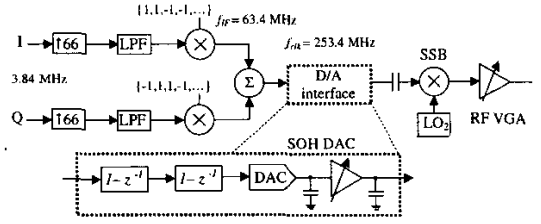

Figure 8. The proposed transmitter architecture which features a SOH DAC.

III. Simulation Results

To establish the feasibility of our architecture illustrated in Figure 8 (which does not require a sophisticated on-chip reconstruction filter or an external IF SAW filter), we present the system-level simulation results. In particular, we demonstrate that the SOH DAC can meet the spurious emission requirements of a W-CDMA transmitter.

Figure 9(a) shows the simulated output spectrum of the transmitter. The noise floor in the W-CDMA Tx band is mainly dominated by the DAC quantization noise (at the 8-bit level). Due to our choice of clock frequency, no digital images will land in the W-CDMA Rx band. Notice that the quantization noise of the DAC in the W-CDMA Rx band is heavily attenuated due to the notch of the $(\sin(x)/x)^3$ rolloff, which is rather advantageous.

The output spectrum at the antenna is found by including the attenuation of the RF SAW (in front of the power amplifier) and the duplexer (after the power amplifier) on the spectrum of Figure 9(a). Displayed in terms of dBc/5MHz, the final Tx spectrum is shown in Figure 9(b). It is shown that our transmitter (which features the SOH DAC) satisfies the spurious emission requirements in various bands (including W-CDMA and DCS).

IV. Conclusion

This research intends to accelerate and enhance the power and performance advantages as we move the digital/analog boundary closer to the antenna in the wireless handset transmitter architecture. A simple digital quadrature up-conversion is proposed for perfect I/Q matching and EVM performance. The task of reconstruction filtering is greatly alleviated by (i) frequency planning and (ii) using a high-order-hold DAC circuit. Simulation reveals that the resulting transmitter could meet the W-CDMA spurious emission requirements with virtually no dedicated reconstruction filtering. This architecture is anticipated to be a good candidate for implementation of very low-power highly-integrated transmitter IC for W-CDMA handset applications.

cumbersome because the channel bandwidth (5 MHz) is narrow compared to the clock rate (253.4 MHz).

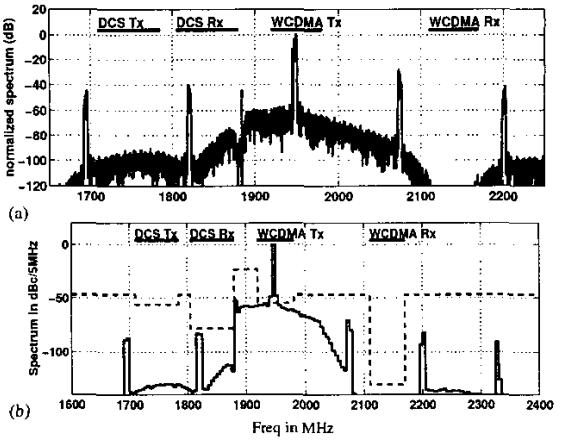

Figure 9. Spectrums, (a) at the output of the transmitter, and (b) at the antenna (after being filtered by the RF SAW and the duplexer).

Acknowledgment

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