A 5 GHZ LOW-POWER, HIGH-LINEARITY LOW-NOISE AMPLIFIER IN A DIGITAL 0.35 μm CMOS PROCESS

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ABSTRACT

A 5 GHz low noise amplifier (LNA), intended for use in a Wireless Local Area Network (WLAN) receiver, has been implemented in a standard digital 0.35 m CMOS process. The amplifier provides a power gain of 9.0 dB with a Noise Figure (NF) of 3.0 dB while consuming 11 mW from a 2.2 V supply and reaches 6.0 dBm at Third Order Input Intermodulation Intercept Point (IIP_3). In this paper, we present a brief analysis of the LNA architecture and experimental results.

***Index Terms*— Radio Frequency (RF) CMOS, analog circuit analysis, amplifier noise, low noise amplifier, MOSFET amplifier circuits, Noise Figure, tuning, impedance matching, linearity, supply voltage.**

I. INTRODUCTION

Portable, wireless, personal-communication devices continue to gain in popularity, and CMOS technology is becoming increasingly popular for the realization of key radio frequency components. [1], [2]. However, the optimum scaling, biasing, and impedance matching of the devices for the realization of the best high-frequency performance in a portable wireless environment remains a challenge, [3], [4]. Applications at 5 GHz have recently become more attractive for WLAN applications, [5], and high linearity and low power dissipation in CMOS technology is especially important for applications in this frequency range. The advantage gained by a digital CMOS process is the economy of integration of different design disciplines on a single wafer fabrication process technology. The potential realized in this research for increased function and performance at reduced costs to the consumer is a driving force for researchers, engineers, and markets.

II. LNA DESIGN

The design of an LNA in an RF circuit requires the trade-off of many important characteristics: Power Gain, NF, and linearity amongst others [6]. This situation forces choices in the design of RF circuits. In the LNA design, the most important RF design attributes are low-noise, moderate gain, high linearity, and stability. Of secondary importance is power consumption and layout design size.

II-A. LNA Design Tradeoffs

Successful RF/analog design depends on design choices for stability followed by the best choices for IIP_3, minimum NF, and Bandwidth. Using the CMOS transistors in a digital process adds an additional complexity for amplifier design. The optimum choice for IIP_3, minimum NF, Power Gain, and Stability in amplifier design using CMOS transistors, is different for each of these RF design attributes. Thus, the optimum capability for each RF design attribute to be realized simultaneously in one application is not achievable [7], [8]. As an example of the broader tradeoffs of combined RF design attributes is the widely known figure-of-merit: the Spur Free Dynamic Range, $SFDR$.

$$SFDR(dB) = \frac{2}{3}(IIP3(dBm) - MDS(dBm)) \quad (1)$$

Remembering that the grounded-source CMOS transistor is marginally stable, tuning or matching choices to optimize other RF design attributes can have the unintended effect of causing the amplifier to oscillate. SFDR depends by definition on IIP_3 and MDS. The definition of Minimum Detectable Signal (MDS) is stated where B represents bandwidth and is set to 20 MHz [9].

$$MDS(dBm) = \quad (2)$$
$$-174(dBm/Hz) + NF(dB) + 10\log(B)(dBHz)$$

where B is the Bandwidth (dB).

As a specific example of trade-offs in this LNA design, notice the SFDR choices shown in Fig. 1. Three choices for SFDR exist depending on which RF attribute amongst IIP_3, NF, or Power Gain is emphasized against the others. In this example, the differences in SFDR performance achievable is clearly shown where the cost of choosing one

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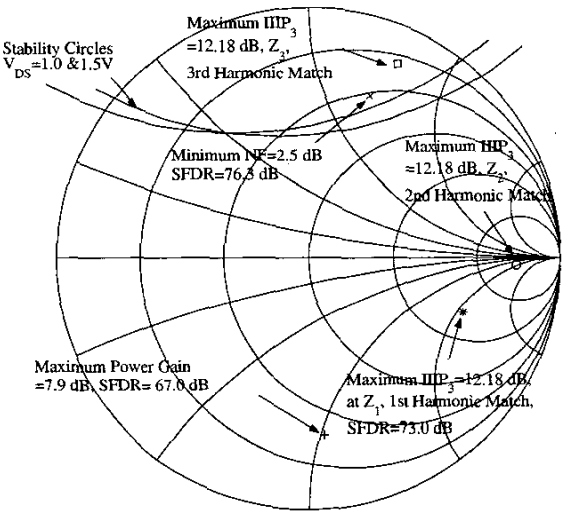

Fig. 1. N200μm Measured Transistor Performance at 5 GHz, V_{DS}=1.5V, I_{DS}=27 mA.

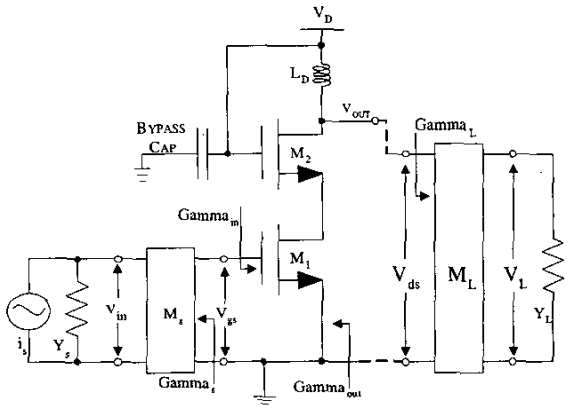

Fig. 2. LNA Cascode MOSFET Circuit Model Including Impedance Tuning.

design attribute over the other can be made for a specific current density. Notice that the minimum NF tuning in Fig. 1 lies where the amplifier would be unstable, thus higher NF would be needed to meet stability requirements. Also, the $IIIP_3$ in Fig. 1 is a multi-harmonic function of source tuning. The optimum Power Gain tuning offers the lowest SFDR. The critical choices regarding trade-off of these RF design attributes is graphically shown so that the tradeoffs for different RF attributes can be made. In the LNA design, a middle point, which compromised all of the RF design attributes was chosen, near Z_{in} = 50 Ω. This choice however did provide acceptable minimum NF, moderate Power Gain, and a high $IIIP_3$ at a low current.

II-B. LNA Topology

LNA topologies occur in many forms with common-gate and common-source designs dominating, [10], [11]. The common-gate configuration has a NF minimum of approximately 3.0 dB as a disadvantage, but does not suffer from the Miller effect. The common-source with inductive degeneration has the advantage of input termination matching with no added resistive noise. However the disadvantage is a larger design area for inductors and the poor inductor Quality Factor, Q. Fig. 2 shows the MOS cascode (common-source/gate) circuit. This provides significant gain with high input impedance and low voltage across M_1, [12]. The bypass capacitor attached to the gate of M_2 provides high-frequency ground, while the inductor on the drain of M_2 provides large-signal bias and resonates with the capacitance of M_2 at the f_o of 5 GHz. The cascode MOSFET, M_2, reduces the Miller effect of a MOSFET common-source amplifier by isolating the output capacitance from the input. By reducing the apparent input capacitance, the performance of the CMOS amplifier at high frequency is maintained. The cost with this arrangement is a small increase in noise and layout area from the additional MOSFET, [13].

II-C. Noise Figure Optimization

As a simplification, the NF of the input MOSFET is considered only to guide an estimate of the upper bound expected. The Noise Factor can then be specified in terms of input currents, $F = \frac{\overline{i_{nt}^2}}{\overline{i_{ns}^2}}$, where i_{nt} is the total input noise current from all sources and i_{ns} is the input noise current due to the source admittance only. The current is given by, (3),

$$i_{nt} = i_{ns} + i_{gr} + i_{sub} + i_g + i_{in} + Y_s e_n \qquad (3)$$

where i_{ns} is the source noise current, i_{gr} is the noise current due to the polysilicon gate resistance, i_{sub} is the input current due to the substrate resistance, i_g, is the induced gate noise current, i_{in}, is the equivalent input noise current due to the drain, Y_s, is the source admittance, and e_n, is the equivalent input noise voltage due to the drain. The noise power is proportional to the mean square of the noise current. So,

$$i_{nt}^2 = \overline{(i_s + i_{gr} + i_{sub} + i_g + i_{in} + Y_s e_n)^2} = \qquad (4)$$
$$i_s^2 + i_{gr}^2 + i_{sub}^2 + \overline{(i_g + i_{in} + Y_s e_n)^2}$$

where $i_{gr} = 4kTY_{gr}\Delta f$ and $Y_{gr} = \omega^2 C_{gs}^2 R_g$. Separation of the noise power terms can be made because the

first three terms on the right are uncorrelated to the others. The correlation admittance is given by

$$Y_c = j\omega C_{gs} + j\omega C_{gs}\frac{g_m}{g_{do}}|c|\sqrt{\frac{\delta}{5\gamma}} \qquad (5)$$

where, α, defines the ratio of gate transconductance to drain conductance, $g_m v.g_{do}$, and equals approximately 0.85. The correlated susceptance is identified based on the above

$$B_c \equiv \omega C_{gs}(1 + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}) \qquad (6)$$

The last three equations are a few of the many steps necessary to gain the following final equation for prediction of NF for a CMOS grounded-source amplifier.

$$F_{\min} = 1 + \frac{R_{gr}}{R_s} + \frac{R_{sub}}{R_s} + 2R_n(G_{opt}) \qquad (7)$$

The final form of the minimum NF is seen in (7) where R_n is the Equivalent Noise Resistance and G_{opt} represents the optimum source conductance for the minimum NF, [6]. The prediction is 2.1 dB of NF for a single interdigitated-gate transistor of 200 m x 0.35 m.

II-D. LNA Design Optimization

The tradeoff between gain, $IIIP_3$, and NF has been introduced in II-A by looking at the SFDR to give a wider graphical understanding of the impact of design tradeoff choices. The specific impedance matching choices made in this design which differ from the best choice for each individual RF design attribute will now be discussed. The optima of three different RF design attributes are seen in the several points in Fig. 1. The $IIIP_3$ is shown across the three harmonics of its optimum match in points labeled Z_1, Z_2, and Z_3 in Fig. 1. The best match in this example for $IIIP_3$ would yield 12.2 dBm. The $IIIP_3$ is a function of triple-valued impedance match conditions on the source and load. In this discussion, the source impedance matching is reviewed only. NF minimum is shown to be 2.5 dB in Fig. 1 and at another impedance match point from the maximum of $IIIP_3$. The two RF design attributes will thus need to be compromised to achieve a impedance match closer to 50 Ω, while not degrading Power Gain significantly. Thus, $IIIP_3$ was lowered to 6 dBm and NF raised to 3 dB minimum, a change of 6 dB and 1 dB from each RF design attribute from their optimum impedance match tuning in this design. Power Gain was stable over the range of impedance match tuning changes or tradeoffs for $IIIP_3$ and NF.

The assumption used in this discussion is that the dominate behavior of the LNA's design is a function of the input tuning for NF. The $IIIP_3$ is a function of both the input and output impedance match tuning and is not addressed in this paper, [6], [14], [15].

TABLE I
5.0 GHz CMOS LNA Performance Comparison

Reference	1	2	3	4	5	This Work
Frequency, GHz	5.2	5.8	5.25	5.2	5.2	5.0
Technology,μm	0.25	0.25	0.25	0.25	0.35	0.35
Supply, V	2.0	2.0	3.0	1.5	3.3	2.2
Power, mW	7.2	20	24	9	26.4	11
Gain, dB	18*	10.0	14.4	17	19.3	9.0*
NF, dB	4.8	3	2.5	2.1	2.45	3.0
IIIP3, dBm		2	-1.5		-6.1	6.0
FOM, dB		-14	-17.8		-22.8	-7.4

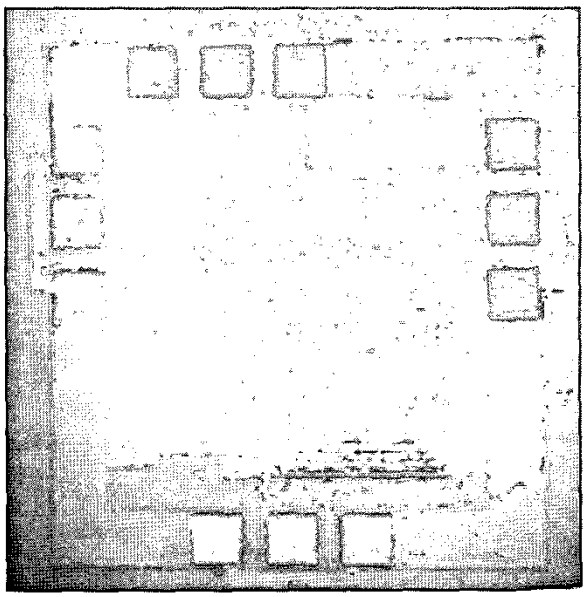

Fig. 3. Microphotograph of 5.0 GHz LNA

III. LNA IMPLEMENTATION

The LNA was implemented as shown in Fig. 2 with the exception of the output buffer not shown to drive the test load. The transistor device widths were chosen to be a ten-fingered, single-sided gate-fed, 200 m x 0.35 m to resonate with the L_D and capacitance of M_2 as seen in Fig. 2. The load inductor of M_2 is a 7-turn square spiral yielding 6.5 nH with a Q of 1.8. The resonant bypass capacitor is a MOSFET capacitor of 0.16 pF. The input inductance is 1.9 nH based on a 3-turn square spiral with a Q of 4.5. A digital CMOS process was used, with the resulting lower performance of the passive elements. This is a well known problem. A microphotograph of the circuit is shown in Fig. 3.

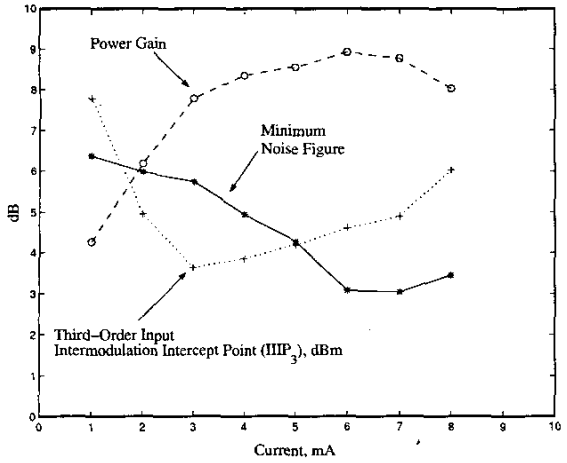

Fig. 4. 5.0 GHz LNA Test Results

IV. EXPERIMENTAL RESULTS

From Fig. 4, the measurement performance at 5 GHz of the LNA can be seen as a function of current. The maximum Power Gain is 9.0 dB and the minimum NF is 3.0 dB. The maximum IIP_3 is 6.0 dBm. The comparative performance is seen in Table 1. The linearity figure of merit, FOM, is defined as

$$FOM(dB) = IIP_3(dBm) - P_{dc}(dBm) - NF(dB) \quad (8)$$

Using the FOM, this design is one of the best ever reported for a CMOS LNA in this frequency range. The experimental measurements were conducted on a Focus Microwaves Load-pull System and a Focus Microwaves Source-pull Noise System at 21 C.

V. CONCLUSIONS

Digital CMOS processes can yield acceptably performing RF LNA circuit designs at 5 GHz for use in WLAN's. This LNA circuit shows high-linearity, moderate power gain, and reasonable minimum NF for an RF front-end receiver is achievable under the constraint of minimum power consumption for wireless 802.11 application. However much care must be spent on the design of the transistors, resonate elements, and the circuit trade-offs to yield good results at 5.0 GHz.

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