Advances in Silicon Semiconductor Device Technology for Radio and Wireless Applications

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Abstract

Silicon technology has progressed over the last several years from a digitally oriented technology to one well suited for microwave and RF applications at a high level of integration. Technology scaling, both at the transistor and back-end metallization level, has driven this progress. This paper summarizes the silicon technology advances associated with radio and wireless applications.

1. Introduction

The need to communicate quickly and reliably is one of the most widespread of human needs, and wireless telephony has exploded in the last decade to fulfill that desire. Roughly 400 million cellular handsets were sold each in the years 2001 and 2002, and the market is expected to grow to nearly a billion phones within the next decade. At the same time, wireless local-area networks (WLANs) are an emerging technology promising untethered communication within computer networks.

The goal of this paper is to highlight the key technological advances in silicon integrated circuit technologies for these RF wireless applications. Based on the improvements in device performance achieved in recent years, it is clear that CMOS or BiCMOS technology, where high-frequency active and passive devices are integrated on a common substrate along with a high level of digital integration, is the preferred medium for these high volume/high performance applications.

2. Substrate and Isolation Technologies

The substrate plays an important role in the performance of an RF-SOC. This is because the desired signal levels are so small, that undesired spurious signals can leak into the sensitive receiver portions through almost any path. Fortunately, many enhancements have been suggested to improve substrate loss and inter-device isolation. These improvements are: *substrate resistivity enhancements, implant blocking layers, and layout dependent improvements.*

Simply increasing the resistivity can provide for a significant improvement in isolation. The resistivity of production Czochralski (CZ) wafers is currently $10 - 20\Omega - cm$, although a new technique known as Magnetic Czochralski (MCZ) has demonstrated resistivities up to $1k\Omega - cm$ [1]. In addition, Float-Zone (FZ) silicon wafers can achieve resistivities of up to $10k\Omega - cm$, although the cost of FZ material is currently substantially higher than that of CZ wafers [2].

Other, more exotic bulk approaches to improving substrate resistivity or isolation have also been proposed for RF-SOC applications. These include the use of Silicon-on-Insulator (SOI) [3], Silicon-on-Sapphire (SOS) [4], Silicon-on-Anything (SOA) [5], porous silicon [6], through substrate vias [7], and bulk micromachining [8].

A more traditional approach to the problem of improving device isolation is the use of grounded "guard rings" that surround the sensitive active devices. The isolation improves with increasing spacing, guard ring width, and substrate resistivity. An example of the use of guard rings to improve isolation is the Bluetooth chip presented by in ISSCC2002 [9]. In this case a 300 m guard ring completely surrounded the sensitive RF portions of the circuit. This enabled the chip to achieve a sensitivity of -82 dBm on a single die containing all of the RF, analog and digital functions.

With a fixed substrate resistivity, a further improvement in isolation can be achieved through the use of a deep low-resistivity n-well placed underneath the active device; when biased to a low impedance and low-noise potential, it acts as an effective shield to signals injected from nearby sources. The addition of a deep well can improve isolation between adjacent devices by roughly 20 dB (from 40 to 60 dB) at 2 GHz [10]. This "triple-well" technology is now a standard option of many sub-0.18 m CMOS processes, using both low resistivity and high resistivity substrates.

3. Transistor Scaling for RF Systems

The key transistor parameters of f_T and f_{MAX} have made astonishing progress in recent years in both SiGe HBTs and MOSFETs, with recently reported values for both devices in excess of 200 GHz [11,12]. The next most important issue is breakdown voltage, which together with

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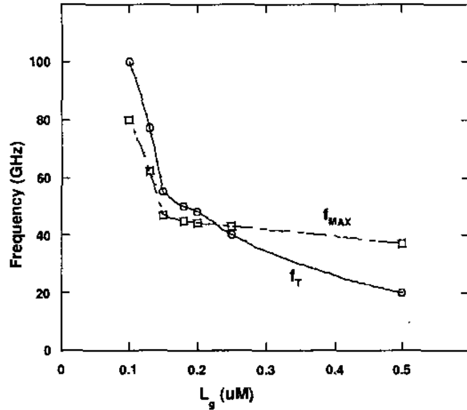

Figure 1. MOSFET speed as a function of gate length [13]. Note that the ratio of f_{MAX}/f_T decreases with decreasing gate length, demonstrating the increasing impact of parasitic gate resistance.

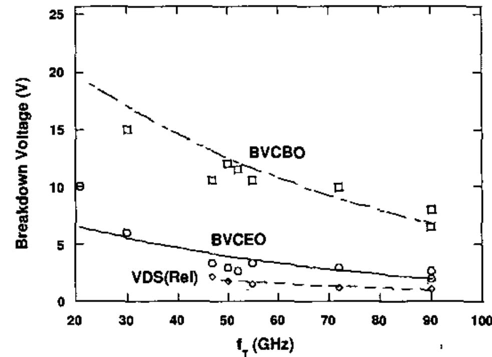

Figure 2. Comparison of voltage limitations of MOSFETS and HBTs as a function of f_T [13, 16].

noise considerations, sets the dynamic range limitation of most circuits. Although Si/SiGe HBT's have historically been leading MOS devices in terms of peak reported f_T, super-scaled MOS devices have recently demonstrated outstanding results as well, and we are now at a point where laboratory results of f_T are nearly comparable. Fig. 1 shows that the *ratio* of f_{MAX}/f_T for the MOSFET has been falling as the speed of the devices rises, in response to the increased gate resistance of the ultra-short gate length in the sub 0.25 m region.

The other key issue for RF applications of scaled transistors is the breakdown voltage of the device, which influences the dynamic range of operation, mostly in power amplifiers in the transmitter section. This breakdown effect is traded-off against the increasing f_T of the transistor, and the $BV * f_T$ product is the key consideration for most high-frequency applications and is a material related constant known as the *Johnson limit* [14]. In the bipolar device, the collector-base junction typically experiences avalanche breakdown first, and the device can be characterized by the collector-emitter breakdown voltage when the base is shorted to the emitter (BVCBO) or when the base is open-circuited (BVCEO). The former is usually larger than the latter, due to current gain in the emitter-base region [15]

When the devices have very shallow doping (as in the high f_T case), the transistors exhibit nonlocal avalanche, and the $BV * f_T$ of the device can exceed its value seen for lower frequency devices [16]. Fig. 2 plots the BVCEO and BVCBO for modern bipolar devices, and the effects of nonlocal avalanching on breakdown voltage can clearly be seen at the higher f_T values, where the breakdown voltage does not change significantly as the f_T increases. In the operation of a power amplifier *circuit*, the device can typically operate at peak voltages in excess of BVCEO, but less than BVCBO, due to the time dependent nature of the carrier multiplication process [17] and the impedances presented at each terminal.

The breakdown voltage mechanisms limiting MOSFET performance are complicated by the diverse breakdown mechanisms, primarily time-dependent dielectric breakdown (TDDB)due to impact ionization in the drain region, gate-oxide rupture, drain avalanche breakdown, parasitic bipolar transistor operation and punchthrough [18]. In many RF applications, the instantaneous dc voltage can significantly exceed the dc voltage, with potentially deleterious consequences. This phenomena has recently been observed to degrade the output power of a 0.18 m CMOS power amplifier over a matter of days of operation [19].

There seems to be a small but significant advantage for the bipolar device in this high voltage regime, which is attributed to the fact that there is a cumulative degradation mechanism when the MOSFET is operated in the weak avalanche range of operation (due to the long term shift in the threshold voltage). By comparison, bipolar devices appear to recover without any degradation in performance from weak avalanche breakdown in the collector-base junction.

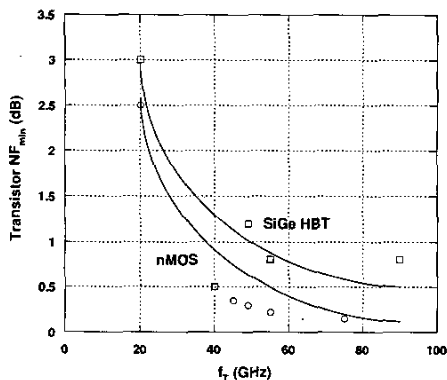

Figure 3. Comparison of reported SiGe HBT and MOSFET minimum device Noise Figures as a function of peak f_T.

4. Small-Signal Noise and Linearity Performance

The microwave noise performance of both bipolar and MOS transistors has improved dramatically in recent years, thanks to aggressive technology scaling that was largely designed to improve digital circuit performance. A comparison of the reported Noise Figure characteristics of SiGe HBT and MOS devices is shown in Fig. 3. The key determinant of Noise Figure performance is the f_T of the device, with MOS devices demonstrating roughly 0.5 dB improvement for a given f_T compared to an equivalent HBT device. However, as Voinigescu *et. al* pointed out, this advantage is difficult to realize in *practice*, because the optimum source impedance for the MOS device is much higher than that of the HBT, making the Noise Figure of a MOSFET LNA very sensitive to source impedance mismatch [20]. One solution to this dilemma is to increase the size of the MOSFET, at the expense of higher power dissipation. In this case, the bipolar LNA would exhibit a slightly lower power dissipation than the MOSFET implementation for a given Noise Figure.

If we examine the case of the higher frequency performance, the linearity is complicated by the nonlinear stored charge effects and the impedances at each terminal of the transistor. These nonlinearities introduce a *frequency dependence* to the nonlinearity. The situation can be simplified if we consider resistive terminations *only* at each terminal of the transistor. As an example, at sufficiently high frequencies, and without avalanche breakdown occurring, the OIP2 of a bipolar transistor is given by [21]

$$OIP2(2f) \approx \frac{4\widehat{f_T}}{\widehat{f_T}'} \tag{1}$$

where $\widehat{f_T}'$ is the derivative of $\widehat{f_T}$ with respect to collector current (in the case of the bipolar transistor). To minimize the second-order intermodulation distortion, the transistor should be designed to have as constant an $\widehat{f_T}$ as possible, and the device will have the highest OIP2 near the peak of the $\widehat{f_T}$ vs. i_C curve.

The OIP3 behavior is more complicated than in the OIP2 case, but some important generalizations can be derived from the analysis of device operation. At sufficiently high frequencies, and when the device is operated at the peak of the $\widehat{f_T}$ curve, the OIP3 of the bipolar transistor is given by [21]

$$OIP3_{HF}(2f_1 - f_2)\ _{\widehat{f_T}'=0} \approx \left.\frac{8\widehat{f_T}}{\widehat{f_T}''}\right.^{1/2} \tag{2}$$

Both the OIP2 and OIP3 results cited above demonstrate that the "ideal" bipolar transistor — defined as one with very low junction capacitances and hence nearly constant $\widehat{f_T}$— will have outstanding high-frequency linearity, and that this intrinsic linearity can improve with future device scaling. As the devices scale to higher f_T, avalanche breakdown in the collector region becomes a significant factor, and can also have a deleterious effect on linearity [22], [23].

5. Conclusions

This paper has outlined the effect that semiconductor scaling will have on RF circuit performance in the coming years. The improvement in device speed (through reduction in lithographic dimensions) will continue to enhance performance for many years, although limitations of gate and/or base resistance are becoming increasingly dominant in the sub-0.1 m regime. At the same time, the dynamic range of the circuits will become increasingly challenged — more so with MOSFET than with HBT technology — because voltage limits are being reduced along with gate dimensions. HBTs appear to have some advantages in this regard compared to MOSFETs, since they can accommodate weak avalanche effects without long-term degradation.

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