ANALYSIS OF OPTIMIZED INPUT AND OUTPUT HARMONIC TERMINATION ON THE LINEARITY OF 5 GHZ CMOS RADIO FREQUENCY AMPLIFIERS

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ABSTRACT

The high-frequency nonlinear distortion of a small-signal CMOS common-source amplifier stage is analyzed as a function of bias, source and load termination impedance, and harmonics at 5 GHz using a Volterra analysis. The predictions closely match measurements over bias, and source and load impedances. The results can be applied to low-power wireless RF circuit design applications.

***Index Terms*— Radio Frequency (RF) CMOS, analog circuit analysis, amplifier distortion, nonlinear circuits, Volterra Series, MOSFET amplifier circuits, tuning, impedance matching, linearity, harmonics, supply voltage.**

I. INTRODUCTION

Portable, wireless, personal-communication devices continue to gain in popularity, and CMOS technology is becoming increasingly popular for the realization of key radio frequency components. [1], [2]. However, the optimum scaling, biasing, and tuning of the devices for the realization of the best high-frequency performance in a portable wireless environment remains a challenge, [3], [4]. Applications for 5 GHz have recently become more attractive for wireless LAN applications, [5], and high linearity and low power dissipation in CMOS technology is especially important for applications in this frequency range. There has recently been substantial development of optimized harmonic impedance tuning strategies for low-noise and power amplifier performance improvement, particularly for bipolar transistor LNA's, [6]–[8], but also for CMOS circuits as well, [9]. These techniques typically rely on optimized second-order interaction to cancel third-order non-linearity effects, and the improvement can be substantial without any penalty in noise or power dissipation. Most of the efforts to date have focused on input harmonic tuning for bipolar circuits, but output harmonic tuning can provide additional benefits and the relative merits of each approach are analyzed at 5 GHz for a CMOS amplifier.

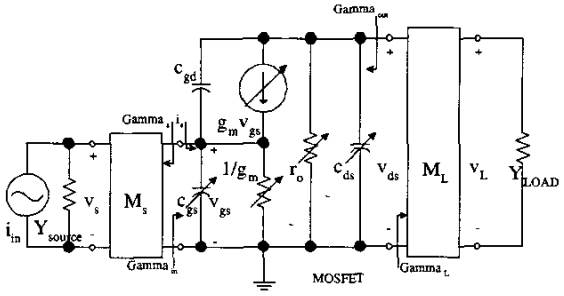

Fig. 1. Small-signal MOSFET Circuit Model Showing Nonlinear Distortion Sources and Tuning.

II. NONLINEAR ANALYSIS OF THE CMOS COMMON-SOURCE AMPLIFIER

The complete nonlinear small-signal model for the MOSFET is shown in Fig. 1, and its resulting nonlinear transfer function is extremely complex. In the most general case, C_{gd} is the only internal element that can be assumed to be linear. We begin with an analysis of the output circuit. The transistor transconductance can be characterized by a nonlinearity of the following general form, [10],

$$i_{gm} = a_1 * v_{gs} + a_2 * v_{gs}^2 + a_3 * v_{gs}^3 + ... \quad (1)$$

where i_{gm} is the small-signal transconductance output current and v_{gs} is the small-signal input voltage. Similarly, the output conductance can be characterized as

$$i_{ro} = g_1 * v_{ds} + g_2 * v_{ds}^2 + g_3 * v_{ds}^3 + ... \quad (2)$$

where the quantities g_1, g_2, g_3, are also functions of v_{gs} and g_1 is the linear drain-source conductance. The output capacitor current can be modelled by

$$i_{c_{ds}} = c_1 \frac{dv_{ds}}{dt} + \frac{c_2}{2} \frac{dv_{ds}^2}{dt} + \frac{c_3}{3} \frac{dv_{ds}^3}{dt} + ... \quad (3)$$

Previous efforts have also assumed that the output impedance of the MOSFET could be modeled as a linear

network, but its nonlinear behavior can have a substantial impact on linearity under some conditions. In the CMOS case, the nonlinearity of the output capacitance and resistances can have a significant effect and we will consider this effect next. By way of illustration, the output voltage in terms of the input voltage at the gate using the Volterra formalism, without the effect of input nonlinearities or feedback, is given by

$$v_{ds} = H_1 \circ v_{gs} + H_2 \circ v_{gs}^2 + H_3 \circ v_{gs}^3 + \ldots \quad (4)$$

and for the circuit of Fig. 1 the following transfer functions can be derived

$$H_1(\omega_a) = \frac{-a_1}{g_1 + y_L(\omega_a) + j\omega_a c_1} \quad (5)$$

and for the second order

$$H_2(\omega_a, \omega_b) = \frac{-\left(a_2 + \left[\begin{array}{l}\left\{g_2 + \frac{c_2}{2} j(\omega_a + \omega_b)\right\} * \\ \left\{\frac{a_1^2}{\{g_1 + y_L(\omega_a) + c_1 j\omega_a\}\{g_1 + y_L(\omega_b) + c_1 j\omega_b\}}\right\}\end{array}\right]\right)}{g_1 + c_1 j(\omega_a + \omega_b) + y_L(\omega_a + \omega_b)} \quad (6)$$

and the third-order transfer function is

$$H_3(\omega_a, \omega_b, \omega_c) = -\frac{\left\{\begin{array}{l} a_3 + (2g_2 + c_2 j\,(\omega_a + \omega_b + \omega_c)) * \\ \left\{\overline{H_1(\omega_a) H_2(\omega_b, \omega_c)}\right\} \\ + \left(g_3 + \frac{c_3}{3} j\,(\omega_a + \omega_b + \omega_c)\right) * \\ \{H_1(\omega_a) H_1(\omega_b) H_1(\omega_c)\}\end{array}\right\}}{\{g_1 + c_1 j\,(\omega_a + \omega_b + \omega_c) + y_L\,(\omega_a + \omega_b + \omega_c)\}} \quad (7)$$

and $\overline{H_1(\omega_a) H_2(\omega_b, \omega_c)}$ is the permutation of H_1 and H_2. described in [11]. The resulting expressions for each of the kernels including input nonlinearities is too involved to present in this paper. However, the effect of linear feedback from C_{gd} alters the final transfer function, Q_n , [12]. The feedback terms of the circuit can be derived as

$$\beta_1(j\omega_a) = \beta_1 = -j\omega_a c_{gd} \quad (8)$$

Next the gain reduction factor is found; i.e.,

$$R(j\omega_a) = \frac{1}{1 + H_1(j\omega_a)\beta_1(j\omega_a)} \quad (9)$$

With these definitions, the overall Volterra Kernels can be expressed including linear feedback, [12].

$$v_{ds} = Q_1 \circ i_s + Q_2 \circ i_s^2 + Q_3 \circ i_s^3 + \cdots \quad (10)$$

where

$$Q_1(j\omega_a) = H_1(j\omega_a) R(j\omega_a) = H_1(j\omega_a) \quad (11)$$

and

$$Q_2(j\omega_a, j\omega_b) = R(j\omega_a)^2 R(2j\omega_a) H_2(j\omega_a, j\omega_b) \quad (12)$$

and

$$Q_3(j\omega_a, j\omega_b, -j\omega_c) = R(j\omega_a)^3 \left[H_3(j\omega_a, j\omega_b, -j\omega_c) - \frac{2H_2(j\omega_a, j\omega_b) H_2(j\omega_a, 2j\omega_b)}{H_1(2j\omega_a)}\right] R(3j\omega_a) \quad (13)$$

With feedback, the Volterra Kernels can be used to predict the IMD_3 as a function of input signal level as

$$IMD_3 = \frac{3|Q_3(j\omega_a, j\omega_b, j\omega_c)|}{4|Q_1(j\omega_a)|} s_i^2 \quad (14)$$

where Q_1 is the complete first-order transfer function and Q_3 is the third-order transfer function. Using the expression for Q_3 and Q_1, linearity estimates from theory can be made and compared to measured results as a function of bias, and harmonic source and load termination impedances. Next, an example of the relationship between harmonic termination impedances and small-signal nonlinearity modelling will be examined to see how the interaction influences the prediction of linearity.

III. INTERACTION OF HARMONIC TERMINATION AND CMOS DEVICE MODELLING FOR PREDICTION OF RF LINEARITY

In this section the role of source and load harmonic termination effects has on third-order input intermodulation distortion, IIP_3, is discussed. Through the non-linearity of the transconductance, output conductance and capacitance will be discussed to develop an intuitive understanding. Estimating these effects requires accurate nonlinear modelling of the device at the output. Although more complicated than in the bipolar case, the expressions for the power series coefficients can be derived from the device models and provide excellent results [12]. The numerator of (7) contains the third-order transconductance term, a_3, the second- and third-order output conductance and capacitance terms. The denominator contains the first order output conductance and capacitance terms, along with the load matching terms.

The load matching term, y_L, of (7) can be described as triple-valued function of the form $y_L \propto (|\Gamma_L|, \prec \Gamma_L, harmonic)$, representing a specific impedance in magnitude and angle on the Smith chart at the harmonics of the fundamental frequency. Because of the interaction, the sum up of each harmonic matching condition in (7) relative to the transconductance, a_3, and output conductance and capacitance nonlinearities causes the increase or decrease in or any other nonlinearity, changes the prediction of linearity from the third-order Volterra kernel, H_3.

Likewise, if the more general case of all the nonlinearities, with their polynomial expansions, is considered,

then their summing up, as a function of a unique set of modelling parameters and termination values at each harmonic, gives the complete conditions upon which the linearity prediction can be calculated. This result immediately suggests a limitation to CMOS amplifier improvement due to harmonic impedance termination techniques. A complete prediction is achieved with linear feedback, derived in (13), and agrees well with measurement for any choice of input or output termination and bias, including harmonic termination. The effects of variations in the load impedance at the fundamental and harmonic frequencies, 2ω, 3ω, on IIP_3 can be seen from examination of (7). Variations in phase at that frequency and its harmonic can affect the IIP_3. Similarly, the magnitude and phase of the output terminating impedance at 3ω can affect the IIP_3. Through the C_{gd} feedback and interaction with the *second- or third-order* nonlinearity at the input, the IIP_3 can also vary. The result is that the IIP_3 is a complex function of the output *and* input terminating impedances at fundamental and harmonic frequencies of 2ω and 3ω. The complete expression provides excellent agreement with the measured results at 5 GHz. This interaction between output and input nonlinearity is different from the bipolar transistor case, where the output impedance network is highly linear, and the C_{bc} is smaller.

IV. EXPERIMENTAL RESULTS

In order to verify the theory, the linearity of 0.35 m NMOS devices in the common-source configuration was measured as a function of dc bias and source and load impedance at the fundamental frequency (5 GHz) as well as the harmonics. This frequency is attractive for wireless LAN applications and is particularly challenging for CMOS technology due to the extreme dynamic range and power dissipation requirements. The peak f_T of these devices was approximately 35 GHz, which is more than adequate for applications in the 5 GHz range. The dc and RF characteristics of the devices were measured to 26 GHz, and the nonlinear coefficients in (1)-(3) were extracted from the measured data as a function of large-signal bias. This data was then used to calculate the fundamental and third-order distortion as a function of the impedances presented to the device at the fundamental and harmonic frequencies as a function of large-signal bias. Fig. 2 plots the change in IIIP3 as a function of second-order and third-order harmonic termination impedance variation, and current for differing device widths (50, 130, and 200 m), currents, and source and load termination impedances (both at the fundamental, and harmonic frequencies). The device current was set to a specific value, and then the source and load impedance at the fundamental and harmonic frequencies were varied with a Focus Load-pull system, and the IIIP3 was recorded at each measurement point.

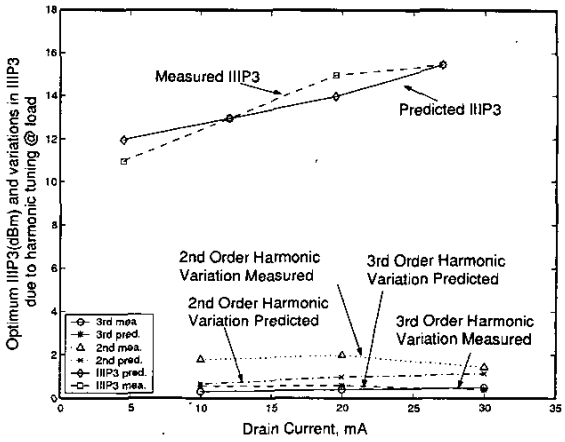

Fig. 2. Optimum IIIP3 and Second- and Third-Harmonic Termination Improvement in IIIP3 vs. Drain Current. V_{DS}=1.5V, P_{in}=-10dBm, Tone Spacing=1.0MHz

This data was then compared against predictions for the same bias and harmonic termination. Each data point in Fig. 2 shows the amount of variation each harmonic termination can have on the IIIP3 at each bias point. As a result, it is a summary of many data points at each bias point.

Several observations can be made from the data and its agreement with predictions. The linearity of the short-channel device in strong inversion is strongly related to dc current, as expected. As can be seen from the lower curves in Fig. 2, a variation in the second harmonic or third harmonic load impedance has an effect on the overall intermodulation distortion, which can be optimized by one to two dB. This is a direct result of the relatively high nonlinearity of the transconductance element, a_3, in comparison to the nonlinearities of the gate-source and drain-source capacitances. This is very different from the behavior of bipolar amplifiers, whose linearity is strongly dependent on the input harmonic tuning effects [6]. This is consistent with previous observations of GaAs MESFET devices, where variations in output harmonic tuning had little impact on the IIIP3 behavior, as well as the results in [13]. Second, the IIIP3 is less affected by variations in the source or load impedances at harmonic frequencies.

A Load-pull plot of IIIP3 on one CMOS transistor is shown in Fig. 3. This measured on a N130 x 0.35 m transistor at 5 GHz using a Focus Load-pull system. The contours displayed are the result of the transistor being measured at over 401 points for IIIP3. The contour lines represent constant contours of 1.0 dB of IIIP3 for that portion of the Smith chart. The square shows the peak IIIP3 for this load-pull run at its fundamental load impedance.

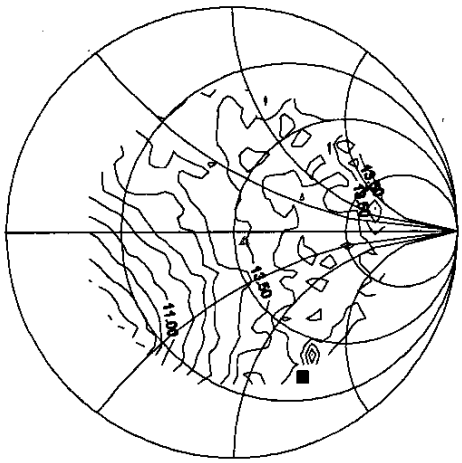

Fig. 3. Intermodulation Load-pull of N130 x 0.35 μm Each line corresponds to a 1.0 dB plateau.

The triangle shows the corresponding fundamental source impedance. The higher harmonic terminations for the source and load are not shown.

V. CONCLUSIONS

The nonlinear performance of a 5 GHz CMOS common-source amplifier has been analyzed and closely matching results predicted, over a broad range of currents, device geometries, and source and load impedances, including *harmonics*. Although algebraically complex, This technique allows the user to identify the key limiting features of the nonlinear operation of CMOS amplifiers, operating in strong inversion, and pick the appropriate bias and terminating impedances to achieve the best performance. The role of harmonic termination impedance (both at the source and load) in predicting CMOS common-source amplifier performance has also been explored, and modest improvements can be achieved using optimized values, although the improvement is shown to be less significant than with bipolar common-emitter amplifiers.

VI. ACKNOWLEDGEMENTS

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