Microwave Device and Circuit Challenges for Next Generation Wireless Applications

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Abstract

The rapid deployment of next generation communications systems both wired and wireless on a worldwide basis creates a unique opportunity for the semiconductor industry. High-speed networks require massive computing power and analog and radio frequency devices with wide dynamic range and bandwidth. The semiconductor technologies required to implement these systems will be highlighted, with particular emphasis on the technologies required to meet the demands of mobile computing applications.

I. Introduction

The explosion of worldwide demand for communication systems has created an enormous and entirely new market for semiconductor devices of all types. As an example, over 400 million wireless handsets are sold annually today, and the annual worldwide market could approach nearly a billion telephones by the end of the decade [1].

This boom has provided an unprecedented opportunity for a variety of new semiconductor device technologies; devices previously deemed too "exotic" for high-volume production are now finding themselves inserted into the most inexpensive portable devices. At the same time, scaled digital CMOS technology is finding increasing use for analog and RF communications applications.

This paper will summarize the semiconductor technology requirements for next generation communications systems, and highlight some trends and challenges for the future. Table I highlights a very top level view of the role of differing technologies in future telecommunications applications.

System	Dynamic Range	Level of Integration	Speed	DC Power	Cost
3G/4G Wireless	Very High	Moderate/ High	1-2 GHz	Very Low	Low
Ad-Hoc Wireless	High	High	2-5 GHz	Very Low	Very Low
UWB	Very High	Medium /High	3-10 GHz	Low	Low
mmW com.	Medium	Low	59-64 GHz	Medium	Low

Table I: Overview of Integrated Circuit Requirements for Next-Generation Wireless Communications Systems

II. Architectures and Systems

An electronic communications system has to contend with a channel that is essentially hostile; its loss is large and time varying, and it often supports multiple users. At the same time, the bandwidth requirements are These aspects of the environment typically result in a great diversity in the amplitude and bandwidth of the received and transmitted signals. How does this fundamental aspect of the medium affect the system design and device requirements

A. Third-Generation Wideband CDMA Wireless

The proposed Third Cellular standard known as Wideband CDMA is one next-generation wireless cellular standard that will be implemented on a worldwide basis over the next decade. The goal

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of third-generation (3G) communications is to provide high-speed data over the cellular infrastructure while providing for improved multipath resolution and diversity compared to existing 2G solutions. The target data rates are 144 kbps for wide-range usage and full mobility, and up to 2Mbps for virtual home service and low mobility. The carrier frequency of the transmit and receive waveforms is approximately 2 GHz. A block diagram of a generic WCDMA handset transceiver is shown in Figure 1.

In this case, the performance challenges require a complex range of semiconductor device technologies, since minimum dc power consumption is an absolute necessity. The handset transmitter power amplifier must transmit a roughly one watt microwave signal with near audio fidelity levels, and dc-rf efficiency as close to 100% as possible. Existing CDMA power amplifiers mostly employ GaAs HBT technology, although GaAs PHEMT technology has also become more popular recently, exhibiting even greater efficiency and linearity [2]. Linearity is an extremely important consideration for 3G power amplifiers, since multiple channels are expected to be transmitted simultaneously through the device, resulting in a very wide dynamic range of the transmitted waveform.

The low-noise amplifier/down-converter and frequency synthesizer sections are typically implemented in a BiCMOS technology for high-gain and dynamic range in the microwave region [3]. The frequency synthesizers can be implemented in BiCMOS or all-CMOS technology. BiCMOS technology is often used for its low-phase noise characteristics, but recent CMOS frequency synthesizers have also demonstrated excellent performance. The digital baseband ASIC is naturally implemented in CMOS. As with the cable modem design, surface acoustic wave (SAW) filters performs the crucial role of channel selection and interference suppression. Once again, one of the key goals of next-generation implementations is the elimination of these bulky and relatively costly devices.

B. Ultra-Wideband Wireless Systems: Device and Circuit Issues

Recent FCC rulings proposed a radiated power limit from UWB devices of -41 dBm/MHz

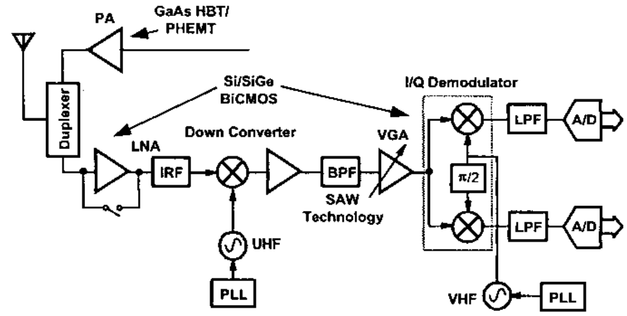

Figure 1: Block diagram of 3G wireless transceiver. A variety of technologies will be required for a complete implementation

from 3.1 to 10.6 GHz. This frequency band co-exists with a variety of kW-level aeronautical and marine radar navigation applications that will present intermittent but severe interference challenges, as well as the well-known commercial use of the 5 GHz ISM bands. The recent introduction of high-power cordless phones in the 5 GHz band will certainly present an increasing challenge to receivers operating in this region. There are several other sources of possible interference in this UWB band, including harmonics of microwave ovens, ignition coils, and harmonics of cellular telephone transmitters operating in the 800 MHz band [4]. Measured data from the NTIA shows that interference events with signal strengths of -20 dBm/MHz can be frequent occurrences between 3 and 5 GHz in a dense urban area, with peaks from airport radar as high as 0 dBm in the 2800 MHz band [5], which is extremely close to the lower UWB frequency limit. Figure 1 is an example of the interference measured from 3100 to 3700 MHz in a typical outdoor Los Angeles environment [5].

As suppression will be required in the UWB receiver in order to provide robust operation. A block diagram of a typical UWB PPM receiver is shown in Figure 2 [6], where a narrowband jammer has been superimposed on the received signal. The first consideration from a receiver perspective is that the gain of the input low-noise amplifier and subsequent analog circuitry does not compress in the presence of a jammer. In this case, the received signal level could easily be as high as -20 dBm, and a typical low-noise amplifier that operates in the 3-5 GHz range in this frequency range and the required input 1dB compression point will dissipate roughly 50 mW of dc power [7].This is considerably larger than a

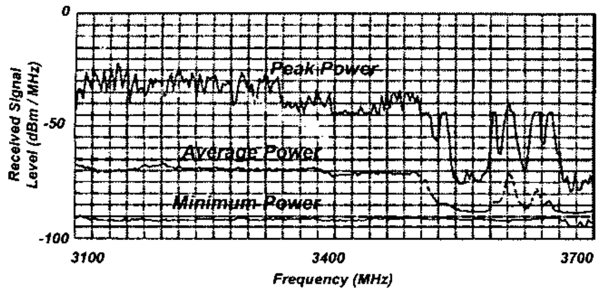

Figure 2: Measured interference in an outdoor urban setting in the proposed UWB band [5].

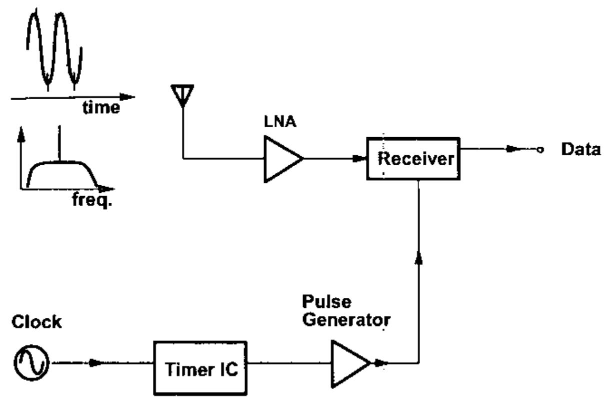

Figure 3. Generic UWB PPM receiver system with superimposed narrowband interferer.

typical cellular or WLAN low-noise amplifier, which have more modest linearity requirements because of their narrow band operation, and illustrates one of the challenges of low-power/low-cost operation in the UWB environment. Since the intended application of these devices is for low-power portable operation, this issue must be addressed at the architectural level.

III. Semiconductor Technologies for Next Generation Communications Systems

In most cases, next generation communications systems will follow the evolutionary path of traditional silicon and III-V technologies. However, within each of these, improved device technologies will create new opportunities for system insertions previously dominated by more exotic approaches.

A. Silicon and SiGe Semiconductor Devices:

Digital CMOS is the tsunami, that created the technological impetus for the communication revolution. Traditional scaling of CMOS technology continues unabated, with production gate lengths now less than 0.10um [8]. The digital VLSI portions of the communications system can ride the CMOS scaling wave for the foreseeable future, and the analog and RF portions of the communications system are also increasingly being implemented in CMOS.

The major issue here is the ultimate limit on scaling and the reduction in dynamic range of MOS devices, since many of the newer systems are actually increasing their dynamic range requirements 3G wireless is a good example [9]. So the challenge will be to maintain the dynamic range of scaled CMOS technology while exploiting its digital capabilities. In addition, digital CMOS foundries have made considerable progress recently in the addition of key passive component technologies - inductors, MIM capacitors, varactor diodes - for RF and mixed-signal applications.

There are applications where power dissipation, high-speed, and dynamic range are crucial in the RF and analog portions of the device once again in 3G wireless circuits - and in these cases, there is a clear role for a Si/SiGe HBT BiCMOS technology. The high transconductance per current and high f_T at low collector voltages [10] makes the bipolar device in a BiCMOS process an ideal candidate for low-power high-performance applications, if its' associated CMOS technology is close to the state-of-the-art performance. Most state-of-the-art BiCMOS foundries have recently announced Si/SiGe HBTs as their baseline bipolar technology, and there seems to be no fundamental reason to prevent the technology from scaling to beyond 300 GHz f_T in the next few years.

B. III-V Devices

After suffering a near death experience in the early 1990s, GaAs technology has found a large and profitable niche serving as key antenna interface circuits (switches, and power amplifiers) for cellular handsets, and, to a lesser extent, as a key technology for fiber-based circuits. The GaAs HBT demonstrated a real knack for linear, efficient, power amplifiers for 2G CDMA wireless applications, and it expected that this will continue for the foreseeable future. This is partly due to the high linearity, gain and breakdown voltage of the device - due to the well-known Johnson limit [11] - and partly due to its intrinsic advantages of single power supply operation compared to a GaAs MESFET. However, GaAs Enhancement-mode PHEMTs have recently demonstrated even better performance, and may prove to be an important power amplifier technology in the future. Silicon HBT power amplifiers have also demonstrated comparable performance to GaAs HBTs in some of these applications [12]. The advantage of III-V technology for high-volume applications other than power amplifiers is less clear, and it is expected that silicon technology - both CMOS and BiCMOS will gradually encroach on the GaAs applications in the lower microwave frequency region (below 5 GHz).

C. New Devices for Communications Applications

One of the most promising new developments in this area is MEMs technology. These devices promise to solve some of the most vexing long-standing problems in communications, including optical switching and low-loss microwave switching in addition to low-loss monolithic filters [13]. In most cases, these devices can be fabricated using silicon VLSI fabrication techniques, and the improvement in performance over traditional approaches can be substantial. However, a variety of fundamental material issues - primarily reliability and yield - need to be solved before these devices find widespread acceptance.

Another very promising semiconductor device technology is GaN-based heterojunction FETs. GaN has a much higher breakdown field than GaAs or InP, and its electron velocity is comparable to those other compound semiconductors. As a result, it may be a nearly ideal device for high power microwave and millimeterwave applications like base stations. Recently, a 9.1W amplifier was demonstrated in this technology at 7 GHz [13].

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