A 16-GHz Ultra-High-Speed Si–SiGe HBT Comparator

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***Abstract*—This paper presents an improved master–slave bipolar Si–SiGe HBT comparator design for ultra-high-speed data converter applications. The latch is maintained during the track stage facilitating quick transition back to the latch stage, increasing the sampling speed of the comparator. Implemented in a 0.5-μm 55-GHz BiCMOS Si–SiGe process, this comparator consumes approximately 80 mW with sampling speeds up to 16 GHz.**

***Index Terms*—Analog–digital conversion, bipolar analog integrated circuits, bipolar integrated circuits, bipolar transistor circuits, comparators, heterojunction bipolar transistors (HBT), high-speed integrated circuits, microwave bipolar integrated circuits, sample-and-hold circuits, ultra-high-speed integrated circuits, very-high-speed integrated circuits.**

I. Introduction

NEXT-GENERATION digital communications systems operating in the 10–60-GHz range will rely on low-cost high-bandwidth receivers operating in multigigahertz range. Analog-to-digital converters (ADCs) will be employed at higher and higher sampling rates with multigigahertz IF bandpass sampled and direct-to-digital systems (see Fig. 1). These ADCs typically have modest resolution requirements, but require extremely wide bandwidths. The comparator in these ADCs plays a crucial role in the overall sample rate and resolution of the converter and must be able to amplify and compare at rates greater than 10 GHz. Increasing the sampling speed and bandwidth while minimizing offsets presents many challenges to the designer. This paper presents an improved design approach to the traditional bipolar master–slave comparator [1]–[6] to reduce the latch time and, thus, increase the overall clock speed of the comparator. The result is a design with a maximum clock rate that is much higher than traditional approaches.

II. Comparator Architecture

A. Review of Existing Comparator Approaches

A traditional latched comparator is shown in Fig. 2. When the *track* signal is high, the input is amplified, and when the *latch* is high, the voltage difference at the output will cause the positive feedback pair to latch, resulting in a digital output signal. One well-known limitation in this design comes at high speeds where significant kickback can be detected at the input due to Q3–Q4 being suddenly shut off. The kickback, due to the back injection of stored base–emitter charge into the base, can significantly distort the incoming signal and limit the performance of higher resolution converters.

A slight modification to this approach adds a current source in parallel with Q_1, which is always on, and will keep the input devices from turning off in the latch mode [5]. This will reduce the kickback seen at the input. For low-power converters, this can help extend the operating frequency beyond initial limits, but further enhancements are necessary if we wish to further extend the frequency of operation.

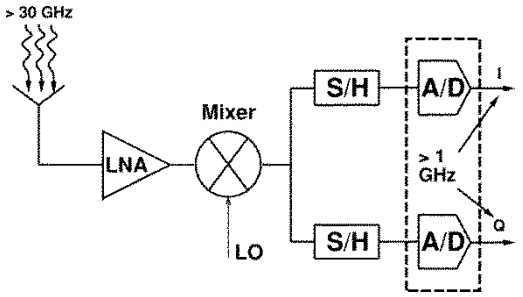

Fig. 1. Millimeter-wave communications receivers will rely on IF sampling system architectures, requiring ADCs operating in the multigigahertz frequency range.

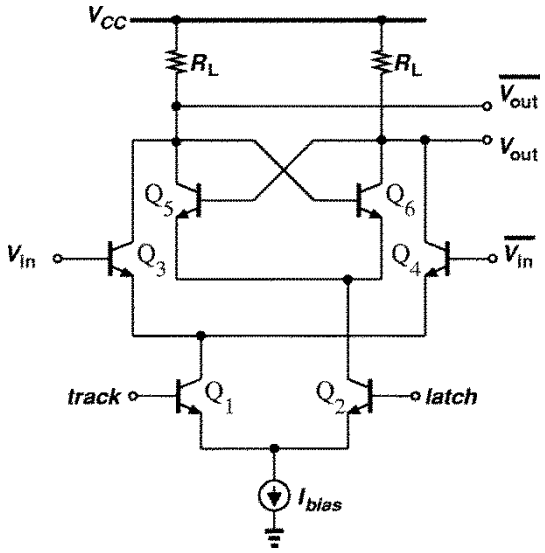

Fig. 2. Traditional track–latch comparator design.

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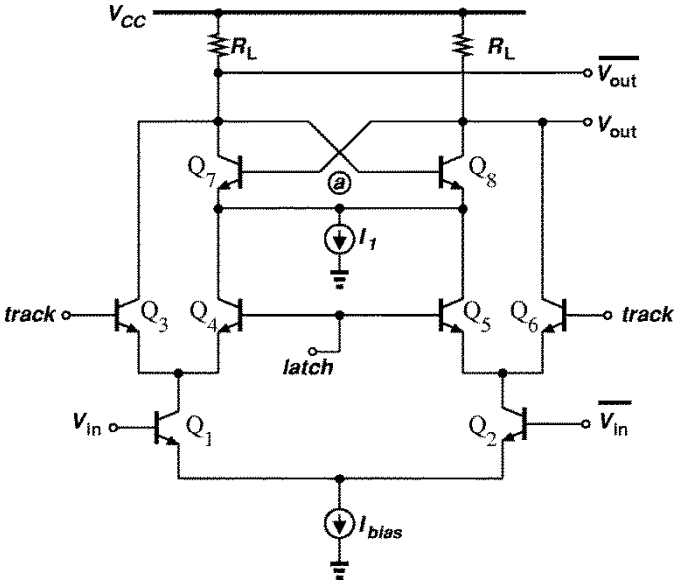

Fig. 3. Improved comparator design with additional current source.

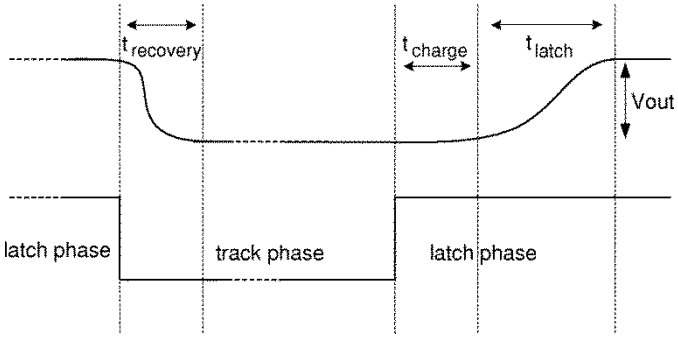

Fig. 4. Delay times during track and latch transitions.

An improvement to the previous design can be seen in Fig. 3 [6]. Here, a current-steering comparator is employed with the input devices Q1–Q2 always on. The bias current $I_{\rm bias}$ is steered by the clock inputs either directly to the output in the track phase or to a cross-coupled pair (Q7–Q8) in the latch phase. This design exhibits improved isolation between the digital output and the input compared with the standard design, at the expense of the increased headroom needed to accommodate the switching devices.

A key speed limitation of this improved design is that when the latch phase is initiated, the base–emitter junctions of the latch, Q7–Q8, will need to turn on and recharge, with the recharge current being provided by the bias current $I_{\rm bias}$ (see Fig. 4). At the absolute maximum clock rates, this junction charging time limits the maximum speed of the comparator; this will be addressed later in this paper.

During the track phase, with $I_1 = 0$, node ⓐ would rise to approximately $V_{\rm cc} - (I_{\rm bias}/2 \cdot R_L)$. Once the comparator moves to the latch mode, this node must drop by $V_{\rm be}|_{\rm on}$. This $V_{\rm be}|_{\rm on}$ is added to the base–emitter voltage at the start of the latch phase and extends the regeneration time of the latch. The relative change in voltage at node ⓐ as a function of current is

$$\Delta V_{\rm be} \approx V_T \cdot \ln\left(\frac{I_{\rm bias}}{I_s}\right) \tag{1}$$

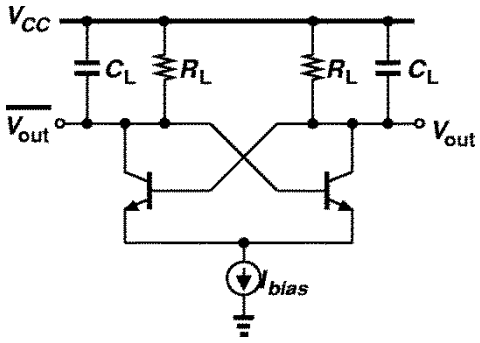

Fig. 5. Comparator configured in the latch mode for calculation of latch-mode time constant.

where $I_{\rm bias}$ is the bias current for the entire comparator. The total time for the latch to produce a digital signal once the latch mode is initiated is the regeneration time. As seen in Fig. 4, the regeneration time is the latch-mode time constant [5] plus the charge time. First, we look at the charge time, which is the time required to charge the base–emitter junctions of the latch transistors. This can be approximated by

$$t_{\rm charge} \approx \frac{C_{\rm be}(V_{\rm be})\Delta V_{\rm be}}{I_{\rm bias}/2} \tag{2}$$

where $C_{\rm be}(V_{\rm be})$ is the base–emitter capacitance and $\Delta V_{\rm be}$ is the base–emitter voltage as described by (1). $t_{\rm charge}$ is approximately 40 ps for our latch transistor with $I_{\rm bias} = 1.0$ mA.

The latch-mode time constant $t_{\rm latch}$ (see Fig. 5) can be written as

$$\begin{aligned} t_{\rm latch} &= \frac{\tau}{(A_{\rm latch} - 1)} \cdot \ln\left(\frac{\Delta V_{\rm final}}{\Delta V_0}\right) \\ &= \frac{C_L}{g_m} \cdot \ln\left(\frac{\Delta V_{\rm final}}{\Delta V_0}\right) \\ &\approx \frac{C_L V_T}{I_{\rm bias}/2} \cdot \ln\left(\frac{2 I_{\rm bias} R_L}{\Delta V_0}\right) \end{aligned}$$

where τ is the *RC* time constant at the output of the latch, $A_{\rm latch}$ is the gain of each transistor, $\Delta V_{\rm final}$ is the desired final voltage difference of the latch, and ΔV_0 is the voltage difference presented to the latch at time $t = 0$. $t_{\rm latch}$ goes to infinity when the voltage difference is zero. Thus, an extremely small input signal will lead to an extremely long latch time. However, the converter is only designed to resolve signals greater than one least significant bit (LSB). Thus, the worst case latch time would be

$$t_{\rm latch}|_{\rm lsb} = \frac{C_L V_T}{I_{\rm bias}/2} \cdot \ln\left(\frac{4 V_T}{A_{\rm pre}{\rm LSB}}\right). \tag{3}$$

The quantity $t_{\rm latch}|_{\rm lsb}$ is computed for ΔV_0 equal to $A_c A_{\rm pre} \times {\rm LSB}/2$, where A_c is the gain of the comparator $(R_L g_m)$ and $A_{\rm pre}$ is the gain of any preamplification before the comparator. The result shows that gain before the comparator helps reduce the latch time by presenting a larger signal to the latch, at the expense of a reduction in bandwidth and increase in power consumption.

During the transition from the latch phase to the track phase, the time that the differential output voltage takes to go from a full digital swing to zero when presented with an input voltage

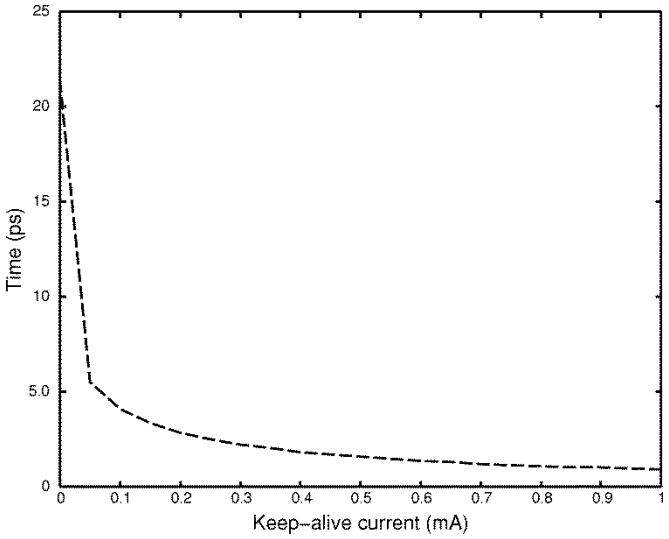

Fig. 6. Predicted variation of $t_{\rm charge}$ in the latch mode with current I_1 from (5).

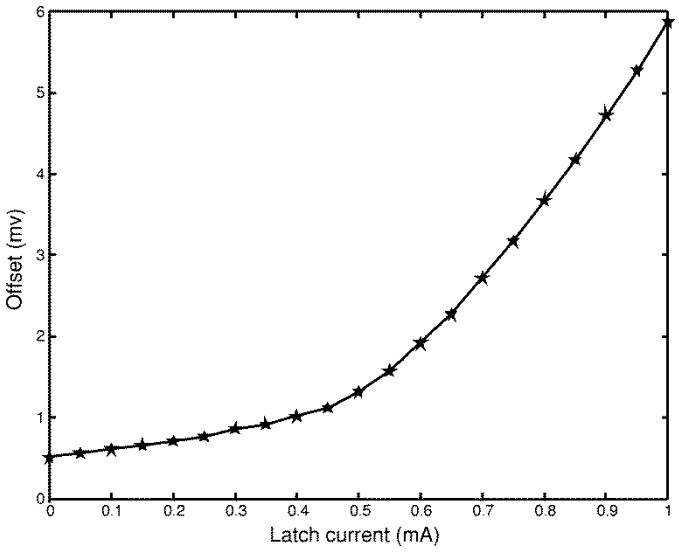

Fig. 7. Offset at comparison point with respect to keep-alive current.

of $-\mathrm{LSB}/2$ is the recovery time. Summing the currents at the output, the recovery time can be written as

$$t_{\rm rec} = R_L C_L \ln\left(1 + \frac{1}{\tanh(\Delta V_0/2V_T)}\right). \qquad (4)$$

For our design $t_{\rm rec}$ is approximately 12 ps for $I_{\rm bias} = 1.0\,\mathrm{mA}$. For low-power comparators, this time can be much longer than the regeneration time, due to the larger output time constants [7]. We were concerned with accommodating ultra-wide bandwidth input signals that lead to a short recovery time.

B. Further Improvements to the Comparator

In an effort to reduce the latch-mode time constant, current source I_1 is added to keep the latch transistors from completely turning off. If Q7–Q8 remains partially on during the track phase of operation, less time is required to fully charge the base–emitter junctions and the overall speed is improved. This small change to the master–slave latch has a profound effect on the overall speed of the comparator.

The time to charge the base–emitter junction, from (2), now becomes

$$t_{\rm charge} \approx \frac{C_{\rm be}(V_{\rm be})(V_{\rm be,final} - V_{\rm be,\ initial})}{I_{\rm bias}/2}. \qquad (5)$$

The results of (5) are plotted in Fig. 6. With I_1 present, the base–emitter junction is precharged, significantly reducing $t_{\rm charge}$ to approximately 7 ps.

Unfortunately, maintaining a small current through the latch devices during the track phase can add a small offset to the input *before* the decision is made. It is important to keep this offset small and provide adequate gain before the comparison occurs to limit its effects. So, there is a fundamental tradeoff between hysteresis and switching speed with this approach that must be carefully assessed by the designer.

As long as I_1 is small during the track phase, the gain of the latch $g_{m7} \cdot R_L$ will be less than unity and the latch will

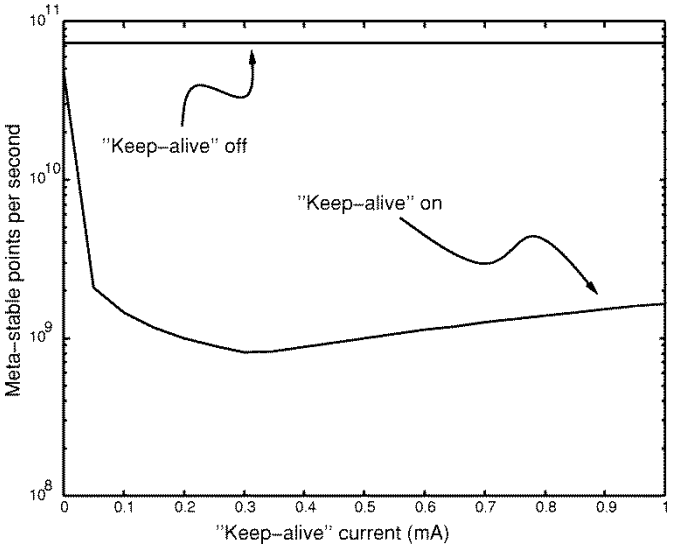

Fig. 8. Simulated number of metastable points per second with a sample rate of 16 GHz. The flat curve is the number of metastable points without a keep-alive device. The second curve shows the number of metastable points per second as a function of the keep-alive current.

increase the overall small-signal gain of the comparator. The small-signal gain peaks when $g_{m7} = 1/R_L$. However, once I_1 exceeds $2V_T/R_L$ during the track phase, the negative conductance of the latch will be greater than $1/R_L$, and all of I_1 will switch to one side of the amplifier output.

In this case, $I_1 \cdot R_L$ will be added to or subtracted from the input during the track phase, depending on the previous decision of the latch. It might be desired to operate the comparator in this region, and the values of R_L and I_1 should be adjusted such that the voltage offset is kept below $A_{\rm pre}A_0 \times \mathrm{LSB}/2$. The improved sampling speed may prove to be more important than the voltage offset created by the latch. This offset will increase with I_1 and eventually may grow larger than the input to the comparator. At this point, the comparator will cease to function correctly and the output of the latch will remain in one logic state with the input never able to overcome the offset and trip

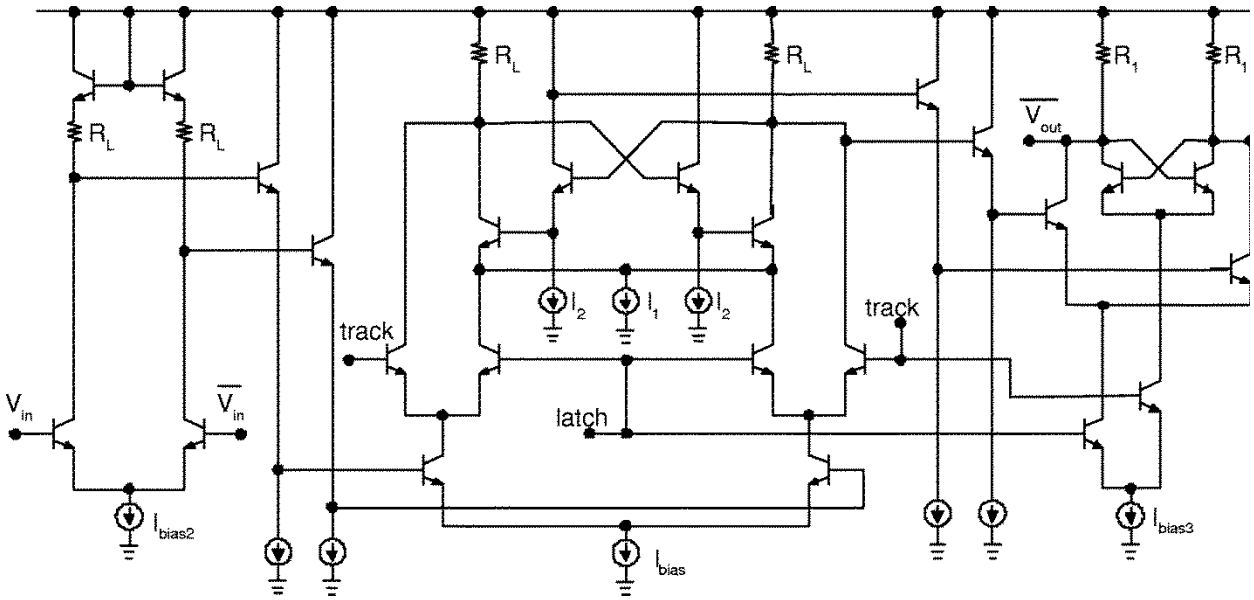

Fig. 9. Input buffer and master and slave comparators.

the latch. Fig. 7 shows the simulated induced offset of the latch with respect to I_1.

III. Analysis of Performance of the Improved Design

A. Comparator Metastability

Signals can exist that are so small that, when presented to the input, no decision is made over the clock period. These signals are called *metastable*; they are not truly stable, since provided enough time, the latch will eventually trip. Previous work [6] has shown that the probability of an occurrence of a metastable point after decision time t_d has elapsed is

$$P(t > t_d) = \exp\left(-\frac{A_{\text{latch}} - 1}{\tau} t_d\right) \tag{6}$$

where τ is the *RC* time constant of the latch, t_d is the time allowed for a decision, and A_{latch} is the open-loop latch gain. Normally for symmetric clocking, and ignoring the latch charging time, t_d will equal $t_s/2$ where $t_s = 1/f_s$ and f_s is the sampling speed of the comparator, but as we can see in Fig. 4, part of each clock period is occupied by the charging time, so $t_d = t_s/2 - t_{\text{charge}}$. As the keep-alive current is increased, the charge time reduces, allowing more time for the the comparator to yield a decision, reducing the occurrence of metastable points. For sample rate f_s, the number of metastable states per second is

$$M_n = f_s \exp\left(-\frac{A_{\text{latch}} - 1}{\tau}(t_s/2 - t_{\text{charge}})\right). \tag{7}$$

M_n is plotted against keep-alive current in Fig. 8. As I_1 increases, the charge time reduces quickly and, thus, the number of metastable points per second dramatically reduces.

The technique that we have proposed here reduces the occurrence of metastable points, since the decision-making time can be substantially decreased if the base–emitter junction of the latch is precharged. From the input buffer to the output of the master comparator, there should be enough gain to minimize instability and overcome the hysteresis produced by the keep-alive current without drastic reduction in bandwidth. There is a gain of approximately 12 dB in the input buffer (see Fig. 9) and another 5 dB in the comparator during the track phase. For I_1 equal to 100 μA, the input offset would be approximately 1 mV, or about equal to that of the transistor mismatches of the comparator.

A wide signal bandwidth will help reduce the tendency for metastability by maintaining signal amplitude at high frequencies. Equation (7) shows that the number of metastable states is directly related to the unity-gain bandwidth of the comparator [6]. To extend the unity-gain bandwidth to its maximum, we place a pair of emitter followers within the loop (see Fig. 9).

IV. Experimental Results

The design was fabricated in IBM's 0.5-μm Si–SiGe BiCMOS process [8]–[9]. The active area was 480 μm$\times$200 μm and the comparator consumes approximately 80 mW with an additional 141 mW consumed in the clock and output buffers used in the test chip. The circuit performance was confirmed using high frequency wafer probes. A die photo is shown in Fig. 10.

Input and clock signals were both differentially matched to 50 Ω. Ultra-broadband off-chip baluns were used to bring the signals on and off chip. The input signal was subsampled with the input frequency 40 MHz higher than the clock frequency. The digital output signal was processed with a logic analyzer state machine clocked at one and a half times the Nyquist rate (just below the maximum rate of the logic analyzer). Without errors, the resultant output signal will be a stream of repeating "100."

Fig. 11 shows the operating of the comparator with an input power of -23 dBm. The comparator performance, shown as the signal-to-noise and distortion, degrades slightly at 9 GHz and stops functioning completely at 10 GHz when the latch remains

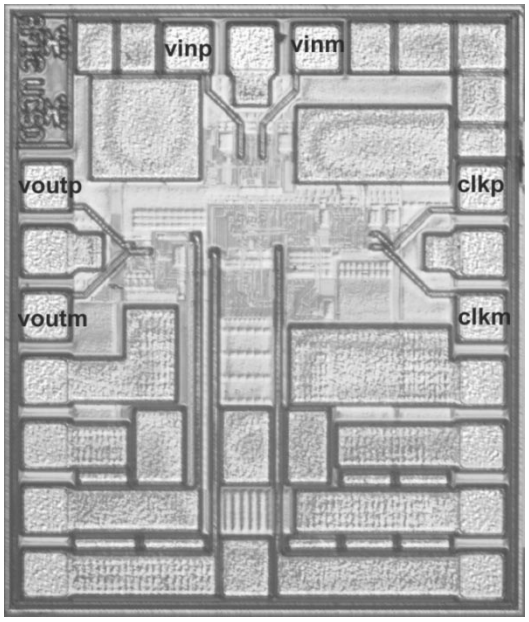

Fig. 10. Die photo of the SiGe HBT comparator.

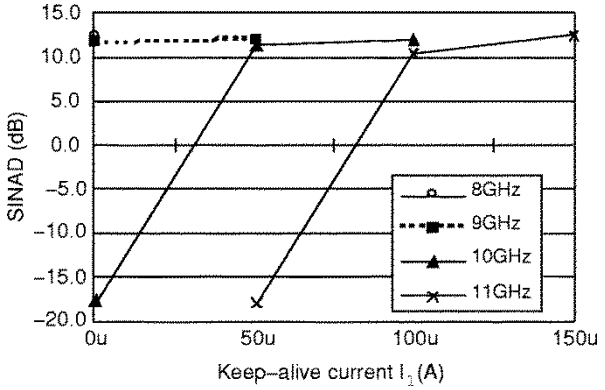

Fig. 11. Comparator performance naturally degrades with increasing operating frequency. With a keep-alive device, the limit of operation is extended.

off in the track phase, but, at 10 GHz, when a small keep-alive current biases the latch, the comparator works again. At 11 GHz, the comparator does not function with zero or 50 μA biasing the latch, but when 100 μA biases the latch, the comparator again functions as predicted.

With a larger input signal, the comparator will operate with a clock frequency of 14 GHz without the latch biased in the track phase. At 15 GHz, the comparator ceases to operate, until the small keep-alive current biases the latch (see Fig. 12). It can also be seen that the performance degrades as the keep-alive current increases, due to the offsets introduced to the input of the latch.

Using the timing function of the logic analyzer, the comparator is clocked at 16 GHz with an input signal of 16.04 GHz. With an input voltage of 20 mV and I_1 turned off, the comparator is unable to function [see Fig. 13(b)]. By increasing the keep-alive current to 100 μA, the emitter–base junction of the latch is precharged and the comparator functions properly [see Fig. 13(a)]. This shows that the maximum operating frequency of the comparator is extended if the latch is kept partially on during the track phase.

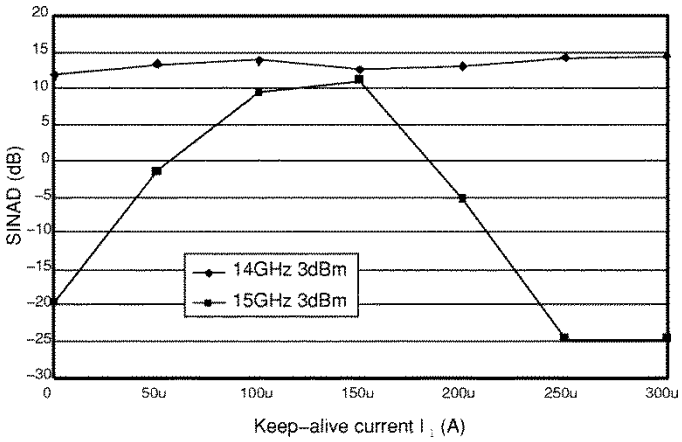

Fig. 12. Extending the frequency of operation. With a small keep-alive device, the comparator will function beyond existing limits.

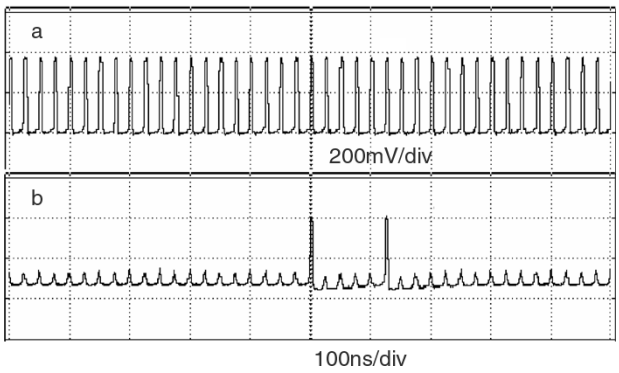

Fig. 13. The 16.04-GHz subsampled comparator output. (a) The keep-alive current is 100 μA, base–emitter diode precharged, and latch functions properly. (b) The keep-alive current is turned off and the comparator is unable to operate.

V. Conclusion

A high-speed comparator has been designed and fabricated with a clock speed in excess of 16 GHz. A keep-alive device is used to reduce the latch regeneration time and extend the frequency of operation.

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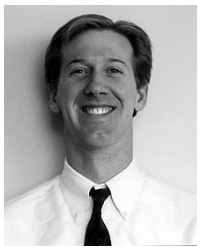

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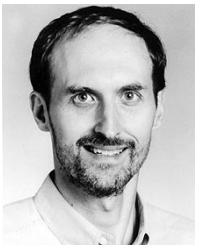

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Dr. Larson was the recipient of the 1995 Hughes Electronics Sector Patent Award for his work on RF MEMs, a corecipient of the 1996 Hughes Electronics Lawrence A. Hyland Patent Award for his work on low-noise millimeter-wave HEMTs, and the 1999 IBM Microelectronics Excellence Award for his work in Si–SiGe HBT technology.