Advances in RF Packaging Technologies for Next-Generation Wireless Communications Applications (Invited Paper)

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Abstract

The performance of a radio frequency integrated circuit can be dramatically affected by the package environment, yet packaging technology has received comparatively little attention compared to IC fabrication technology or RFIC design. This paper summarizes the key developments and trends in RFIC packaging, with particular attention to improvements in plastic package design, low-temperature co-fired ceramic (LTCC), flip-chip approaches, and system-in-package (SIP) implementations.

1. The Role of Packaging in RFIC Applications

The wireless industry is undergoing tremendous growth, spurred in part by small, low-cost Radio Frequency Integrated Circuits (RFICs). The simplest RFICs are designed to perform a single, discrete function, such as amplification or mixing. These chips are usually less than one square millimeter in area, and require fewer than a dozen connections to off-chip circuitry. More involved RFICs can contain complete receive and/or transmit chains into the total RF portion of a radio. These transceiver chips require several dozen high-frequency I/O connections to the printed circuit board (PCB). Table 1 contains a brief list of typical frequencies used by RFICs.

Table 1. Selected RF and Microwave Frequency Bands for RFIC Applications.

Designation	Frequency (GHz)
Cellular	0.9
GPS	1.5
PCS	1.9
3G Cellular	1.9-2.2
WLAN	2.4, 5-6
UWB	3-10
Direct Broadcast Satellite (DBS)	11-12
mmW comm.	60
Vehicle Anti-collision Radar	77

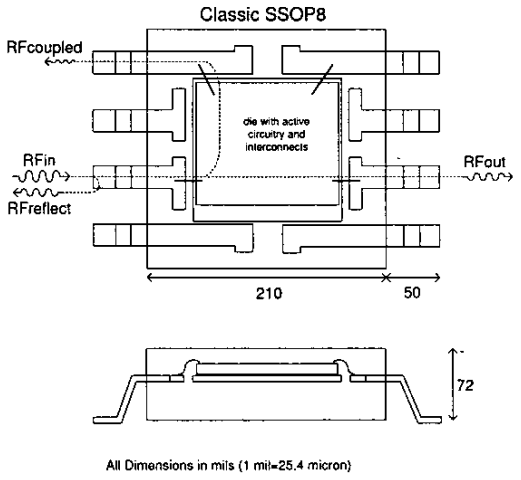

Figure 1. SSOP8 with signal paths through the package and die. Only one coupled path is shown.

The recent trend in new commercial frequency allocations is to higher frequencies. For instance, 5 GHz WLAN and 12 GHz DBS have all been commercially exploited [1]. This has rendered the old design approach of emphasizing the mechanical characteristics of packages with disregard of the RF performance obsolete. Any new package design must consider RF performance of equal priority to mechanical concerns, since lead frame parasitics can cause the package to seriously degrade RFIC performance, if not render the chip unusable.

The ideal package creates a transparent link between the printed circuit board signals and the silicon chip. Any deviation from the ideal package causes the input signal to be degraded. This degradation manifests itself in three ways: excessive Insertion Loss (IL), insufficient Return Loss (RL), and pin-to-pin isolation. Figure 1 illustrates the classic 8-pin Shrink Small Outline Package (SSOP). The RF input signal energy is either reflected, transmitted, or coupled throughout the die and leads. In practical applications all three signal paths exist in varying degrees of magnitude.

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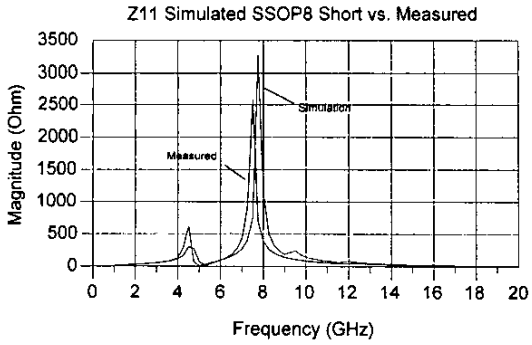

Figure 2. Comparison of simulated and measured result of "shorted" (with bond wires) SSOP8 package. Note the strong 8 GHz resonance, which makes the "short" appear as an open-circuit.

As an illustration of the type of high-frequency problems that can occur with even a simple SSOP package, Figure 2 shows the measured and EM simulated performance of an SSOP8 when the input is shorted to ground through a bond wire interconnect [2]. Z_{11} rises very dramatically to due to the internal inductive reactances in the package, and exhibits a very strong resonance at 8 GHz. Clearly, operation of the package at these frequencies would be very difficult.

This paper will highlight some of the technological challenges that are required to extend the frequency range and functionality of RFIC packages, while keeping costs low for high volume consumer applications. At the same time, the level of integration of these systems is continuing to rise dramatically, and we will also discuss techniques for "system-in-a-package" integration.

2. Traditional Plastic RFIC packages

Plastic package technology has been the "workhorse" of the integrated circuit industry for many years, and this will continue for the foreseeable future. This is due primarily to the low-cost and relatively high performance of the technology. Higher performance ceramic leaded packages have been developed for high performance applications, such as Direct Broadcast Satellite (DBS) service (12.2-12.7 GHz) and Local Multipoint Distribution Service (LMDS) (24-32 GHz) [1, 3]. A four-lead ceramic package has an in-volume cost of roughly $ 5 per package [4], while plastic leaded packages cost approximately $0.01 per lead in-volume [5]. Traditional ceramic packages are thus significantly more expensive than plastic approaches.

The package families listed in Table 2 are a general summary of the state of traditional packaging and its RF performance. Figure 3 illustrates the outline of the packages of Table 2. The In-line package types such as Plastic Dual In-line Package (PDIP), Ceramic Dual In-line Package (CERDIP), and Single In-line Package (SIP) are useful for die in the 8-20 I/O range that require through-hole mounting. The Small Outline (SO) packages in J-bend leads (SOJ), C-shaped leads (SOC), Shrink SO body size (SSOP), and Miniature SO body size (MSOP) are smaller than the In-line types and are surface mountable. For I/O leads greater than 16, the Plastic Quad Flat Pack (PQFP), Plastic Leadless Chip Carrier (PLCC), and Ceramic Quad Flat Pack (CERQUAD) are more appropriate. The most recent developed packages for use in high pin count (> 20) applications are the Bump Chip Carrier (BCC) and the Ball Grid Array (BGA). Further details on package types can be found in [6–8].

Table 2. Package Families and Characteristics

Package Family	**Examples** (GHz)	f_{max}
In-line	PDIP, SIP, CERDIP	2
Small Outline	SOJ, SOC, SSOP, MSOP	5
Quad Surface Mount	PQFP, PLCC, CERQUAD	3
Grid Array	BCC, BGA	7[a]

[a]The Return Loss peaks to 18 dB at 3 GHz then drops below 20 dB to 7 GHz.

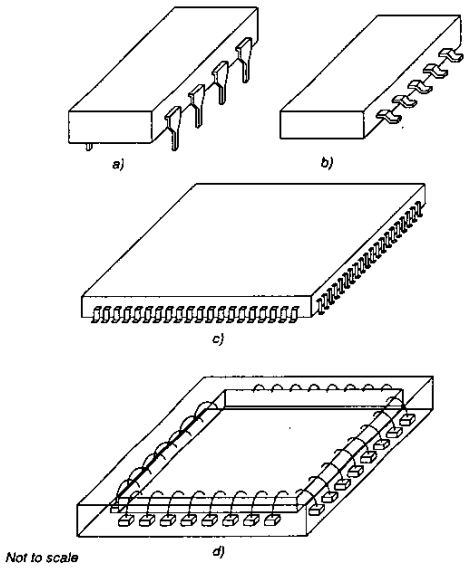

Figure 3. Four categories of plastic packages: a) DIP; b) SO-type; c) QFP; d) Bump Chip Carrier (BCC).

One crucial aspect of the use of these packages is obtaining an accurate equivalent circuit model, for use in the overall IC design process. The various deleterious aspects

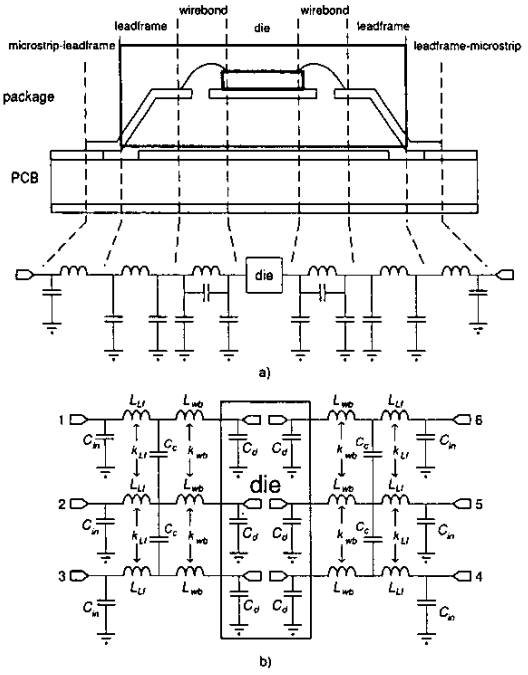

Figure 4. Traditional SO-type leaded package: a) Cross-section showing the origination of package parasitics; b) Simple electrical model of six leads including nearest neighbor coupling.

of the package performance can be partially overcome if they are known, and can be modelled, during the design process. The lead frame equivalent circuit is usually modelled as a lumped circuit array where every lead and bond wire is coupled to every other lead and bond wire in an RLCM matrix [9–18].

Figure 4(a) is the cross section of a SO-type plastic leaded package. Included in the diagram is the outline of the plastic body, lead frame, bond wire, and die. In Figure 4(b), a simplified electrical representation of the SO package is given. For simplicity, only six leads are shown.

The capacitance C_{in} is created between the lead frame solder pad and the backplane ground. It is dependent on the dielectric constant, thickness of the PCB, and solder pad area. The quantity L_{Lf} is the lumped inductance of the lead frame conductor and captures some of the PCB to lead frame parasitic inductance. The inductance L_{wb} is the lumped inductance of the bond wire. C_d is the bond pad capacitance where the bond wire attaches to the die. The terms k_{Lf} and k_{wb} are the magnetic coupling coefficients between the lead frame pins and the bond wires, respectively. There is also a capacitive coupling term C_c between pins. It should be noted that all pins in a package couple to every other pin, but coupling between nearest neighbors are usually the most dominant.

We will concentrate on models of the lead frame and wire bond inductances first, since these typically cause the greatest problems. We will then show how the performance of the package can be improved through redesign of the lead frame in some cases.

2.1. Lead Frame Inductance

The lead frame inductance is directly dependent on the length of the conductor and the cross sectional area, i.e. a short thick line has less inductance than a long thin line. A formula that has proven to be accurate at low frequencies is given by [19]

$$L(\mu H) = 0.002l\left(\ln\left[\frac{2l}{(w+t)}\right] + 0.50049 + \left[\frac{(w+t)}{3l}\right]\right) \quad (1)$$

where l, w, t are the length, width, and thickness of the conductor in cm, respectively.

One can see that scaling the size of the lead shorter in length will directly reduce the series inductance of the lead frame. From an RF perspective, this accounts for the motivation to move to smaller SO type packages (SOIC → SSOP → MSOP). Typical self-inductances of lead frames are approximately 0.9nH/mm [20], and are fairly insensitive to small changes in the physical dimensions of the package itself.

The *mutual inductance* between adjacent pins and bond wires increase the total reactance of any pin, since the inductive reactances of nearby pins add to the total reactance. In addition, it leads to serious coupling between adjacent pins due to the induced currents in the coupled inductors, through the well-known relation

$$V_L = sLI_1 + sMI_2 \quad (2)$$

where V_L is the voltage across the inductor, L is the series inductance of the lead, I_1 is the current through the inductor, M is the mutual inductance between adjacent conductors, and I_2 is the current through the coupled inductor.

The coupling factor k is then related to the mutual inductance by

$$k = \frac{M_{12}}{\sqrt{L_1 L_2}} \quad (3)$$

where L_1 and L_2 are the self inductances of either the lead frame or bond wires. If $L_1 = L_2$, then the coupling coefficient is directly proportional to the mutual inductance and inversely proportional to the self inductance. Increasing the self inductance of the lines *decreases* the magnetic coupling (if the mutual term is left constant), thus reducing the coupling between lines and improving the isolation. However, this would increase the series reactance of the lead and degrading RL and IL.

The mutual inductance of a conductor can be modelled to first order by [21]

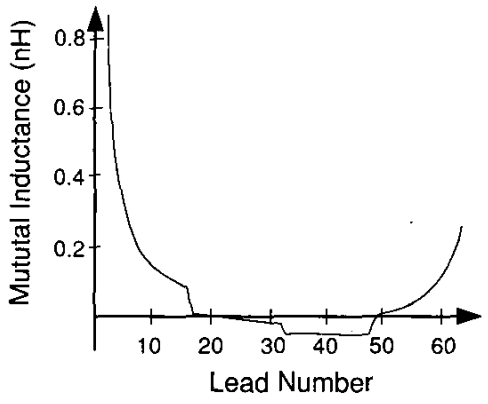

Figure 5. Mutual inductance in (nH) between the pins of a TQFP64 package [20]. Note that the mutual coupling becomes *negative* on opposite sides of the package.

$$M_{12}(\mu H) = 0.002l\left(\ln\left[\frac{\frac{l}{d}+\sqrt{1+\frac{l^2}{d^2}}}{-\sqrt{1+\frac{d^2}{l^2}}+\frac{d}{l}}\right]\right) \quad (4)$$

where l and d are the length and distance apart of the conductors in cm, respectively. The direct dependence of length is again seen in modelling the magnetic effects of current carrying conductors.

The mutual inductance between any two pins of the lead frame has been extensively modelled, most recently by [20] for the case of a TQFP64 pin package, which was optimized for use in a GSM transceiver application. The results of the mutual inductance model are shown in Figure 5. It is clear that the most nearest neighbors exhibit the greatest mutual inductance, and that the mutual inductance drops off rapidly as the bond wire separation grows. It is also interesting to note that the mutual inductance becomes slightly *negative* in case where the angle between the bond wires substantially exceeds 90 degrees.

2.2. Wire Bond Inductance

Despite their large self- and mutual inductances, bond wires continue to be the dominant technique to connect an RFIC to the package. Bond wires are very robust and inexpensive, and able to tolerate die thermal expansion and placement uncertainty. However, their inductance creates significant challenges for RFIC design, as well as some unique opportunities. For example, bond wire inductors have been used as resonators in RF VCOs [22] as well as matching elements in monolithic distributed amplifiers [23].

Bond-wire inductance has been extensively studied recently, and there is substantial literature published on the value of inductance, mutual inductance and capacitance. The wire bond inductance is dependent on the length of the bond wire and the cross sectional area. Most bond wires are 25-30 μm in diameter and between one and two millimeters in length. An approximate formula that has proven accurate at low frequencies is given by [21]

$$L(\mu H) = 0.002l\left(\ln\left[\frac{2l}{\rho}\right] - 0.75\right) \quad (5)$$

where l and ρ are the length and radius of the bond wire in cm, respectively.

More accurate models of bond-wire inductance require full 3D simulations, and account for the curvature of the wire bond, as well as the height above the ground plane. Values of approximately 1 nH/mm are commonly used as a "rule of thumb," but more accurate results are often required.

In this case, the results of [24] are a useful guide for modelling of bond wire inductance, and the simulated results for bond wire inductances a function of length are shown in Figure 6. In this case, a full finite-difference time-domain (FDTD) simulation was performed on the structure, and a simulation was performed to 50 GHz. The "one nH/mm" rule was confirmed, but there is a significant effect on the inductance as the distance to the ground plane was varied. In addition, the effect of parallelling two bond wires ($200\mu m$ apart) was also investigated. In this case, the equivalent series inductance drops by approximate 30 percent when two bond wires are in parallel. In order to accurately model the inductance to very high frequencies, a second-order coefficient of inductance had to be added to account for the decreasing inductance at higher frequencies, i.e.

$$L = L_0 + L_2 f^2 \quad (6)$$

From [24], the value of L_2 could be approximated by $-0.1pH/(GHz^2mm)$ for a single bond wire, and approximately $-0.06pH/(GHz^2mm)$ for a double bond wire.

2.3. Improvements in Lead Frame Design

The inductances associated with the lead frame naturally suggests that the package performance could be significantly improved if the lead frame could be formed into a transmission line-like structure with the appropriate characteristic impedance. This would increase the bandwidth of the resulting package significantly, and minimize reflections at the various transmissions into the package.

This approach was recently adopted to increase the useful bandwidth of an SSOP-8 package to well over 10 GHz [25]. In this case, the package lead frame was modelled as an Embedded Coplanar Waveguide with Finite Grounds (ECPWFG) structure, and the characteristic impedance was directly calculated. The lead frame design was slightly modified to present a 50Ω characteristic impedance to the PC board. The resulting package exhibited improved performance compared to the standard SSOP-8 package, with return loss greater than 20 dB to 11 GHz, and insertion loss less than 1 dB. This type of

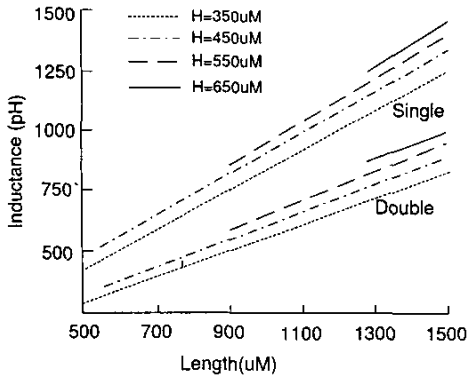

Figure 6. FDTD simulated bond wire inductance as a function of length for single and parallel (spacing = $200\mu m$) cases [24]. The inductance falls as the bond wire separation from the ground plane decreases.

"engineered" lead frame design holds great promise for increasing the performance of RF packages at higher microwave frequencies.

2.4. Flip-Chip Technology

Flip-chip technology offers an opportunity to reduce the inductance associated with mating of the IC die to the package or substrate. The flip-chip solder bumps are typically fabricated from alloys of indium and lead, although "lead-free" stud bumps have also become popular. In many cases, the inductance of the solder bump can be reduced to approximately 50 pH, significantly less than the 1nH/mm of a bond wire. Other advantages of this approach include the ability to place these connections near the center of the die, improving the flexibility of the system partitioning and reducing the ground inductance in the interior portions of the chip. Flip-chip approaches are also well suited to ball-grid array packages, which themselves exhibit very low inductance, as shown in Figure 8 [26]. The combination of the ball-grid array package and flip-chip represents a significant improvement in microwave performance over the traditional leaded-package approach with bond wire attachment.

The major drawback limiting flip-chip today is the increased cost — roughly 2-3X the cost of an equivalent wire bond attachment on a per-pin basis. In addition, the bond wire pitch can be substantially less than that of an equivalent flip-chip pitch, and staggered bond wires can reduce the wire pitch even further.

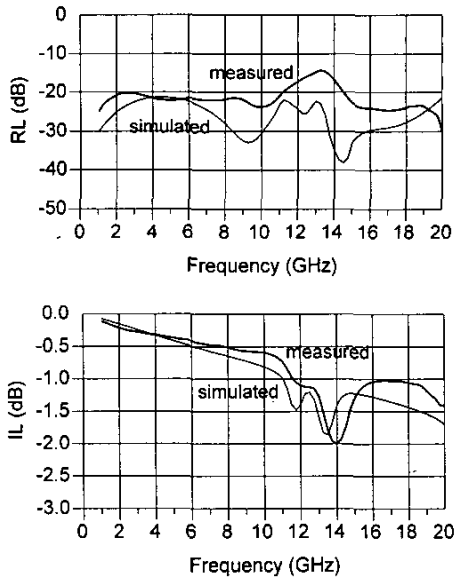

Figure 7. Simulated and measured return loss (RL) and insertion loss (IL) response for improved SSOP8 ECP-WFG Thru package [25]. Note that the return loss exceeds 20 dB to 11 GHz, and the insertion loss is less than 1 dB over this frequency range.

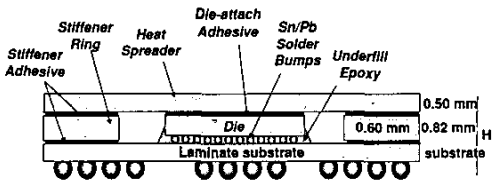

Figure 8. Cross-section of flip-chip die mounted on BGA, with integrated heat spreader and stiffener ring. The flip-chip technology provides a low-inductance connection to the package [26].

3. Low-Temperature Co-Fired Ceramic (LTCC) Packaging

Low-Temperature Co-fired Ceramic (LTCC) material provides an alternative low-cost packaging approach for RFICs [27]. LTCC layers are built-up on individual layers of flexible ceramic tape (so-called "Green Tape") and are then pressed together and "fired" at temperatures approaching $900^{o}C$. The resulting multi-layer ceramic structure exhibits relatively low loss and shrinkage, and high-performance passive microwave components can be essentially built-in to the substrate, since high conductivity metals like gold and silver can be employed due to the low firing temperature. This ability to integrate the high-performance passive components into the package in a low-cost way is the compelling attribute of this approach.

This technology was originally developed for military applications, but has recently found its way into a variety of commercial products. For example, a WCDMA downconverter was demonstrated by Mitsubishi [28], which used the capabilities of LTCC to great advantage. In this case, an even-order sub-harmonic direct-conversion receiver was implemented, as shown in Figure 9. Several key passive components, including the interstage filtering, hybrid phase shifter, and power splitter, were all implemented on the LTCC substrate. The resulting SiGe HBT die size was very small, since many of the passive components were implemented on the LTCC, and flip-chip technology was employed to connect the die to the board with low parasitic inductance. The overall dc current requirements were only 12 mA for the complete downconverter. Another example of the use of the creative use of LTCC is a Bluetooth receiver implemented by Ericsson, where the flip-chip assembly was employed, and transmit/receive filter and baluns were implemented on the substrate [29].

The key limiting feature of LTCC is still related to issues of manufacturability and cost. Uneven shrinkage of the tape during firing has historically been a problem, although this has improved in recent years [30]. Another factor limiting adoption of LTCC is that the performance of passive devices on IC dies is itself improving dramatically; inductor Q's are improving due to thicker metallization and the use of copper and MIM capacitors are shrinking in size due to the use of thinner dielectrics. The relative attractiveness of LTCC technology requires constant re-examination in light of these ongoing improvements.

4. System-in-Package (SIP) Solution

The needs for increasing levels of integration are driving packaging technology towards ever more creative solutions for combining RF and digital functions in a common package. The traditional approach to this challenge is to combine all of the functions — RF, analog/mixed signal, and digital — onto a common integrated circuit substrate.

Although a fully integrated approach can lead to an attractive solution in some cases, it is often less than optimum from a system perspective. If the most advanced digital technology is employed for this "single-chip" solution, then the performance of the RF and analog components are compromised due to the lack of high performance passive devices and immature device models. In addition, the analog dynamic range performance of the most advanced CMOS digital devices is often compromised in the effort to reduce the gate length to its absolute minimum [31]. Conversely, if the IC technology is chosen to optimize the performance of the RF/analog circuits, then the performance of the digital system is equally degraded. Co-integration of digital and RF/analog functions on a single IC die can lead to serious contamination of sensitive analog nodes with digital switching noise. Elaborate guard ring and isolation approaches are often required in order to reduce the problem to a manageable level [32].

Several novel solutions have been employed recently to allow both the RF/analog *and* the digital IC processes to be separately optimized, by placing two different die into a common package; this can involve either placing the die side-by-side in a package, or stacked on top of each other. These "System-in-a-Package" (SIP) approaches provide an alternative to a "System-on-a-Chip" (SOC) approach without an excessive cost or form-factor penalty.

As an example of the former approach, a complete Bluetooth solution in a $0.25\mu m$ RF-CMOS process is reported in [33]. There are two major components to a complete Bluetooth IC solution: the radio blocks and the baseband processor. Combining them all onto a single die can degrade the performance of the RF receiver, and so separating the digital and RF functions onto separate dies is an attractive approach. The Bluetooth RF-SIP was packaged in two-die configuration consists of a RFIC die and a Baseband IC die. The package used is 8x8 mm SS-BGA. The complete solution required only 14 external passive components and a crystal. Figure 10 shows the microphotograph of the two-die bonding configuration, where the logic die (digital IC) and the radio die (RFIC) are bond wire connected. The bond wire "bridge" between the RF and digital die adds little to the cost of the package, but increases the flexibility of implementation enormously. Multiple versions of the digital IC can be produced for a given application, without having to re-design the RF/analog blocks each time.

"Stacked" die approaches have also become popular recently for integrating multiple large digital chips in a single package, and it is expected that these approaches will also become popular for highly integrated RF transceivers where both digital and analog functions are required in a small area. In this case, improved die thinning techniques and fine pitch wire bonding equipment allows multiple die to be stacked on top of each other with acceptable form factor and acceptably short bond wire length. A cross-section of a two-stack die is shown in Figure 11.

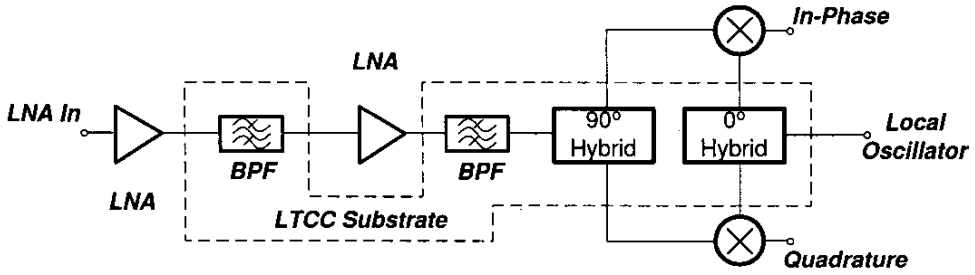

Figure 9. LTCC-based WCDMA RF direct conversion receiver [28]. Most of the passive elements were realized on the LTCC substrate, and the resulting SiGe BiCMOS die was flip-chipped onto the substrate.

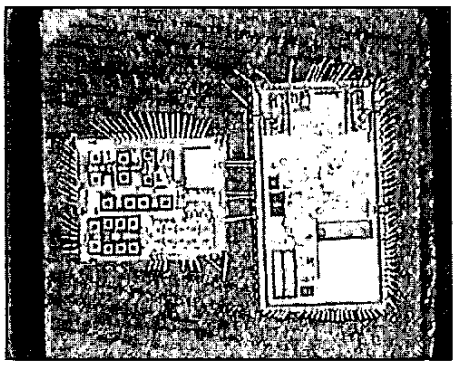

Figure 10. Die photograph of two-die Bluetooth solution. The die on the left contains all of the radio functions, and the die on the right contains the baseband processor [33].

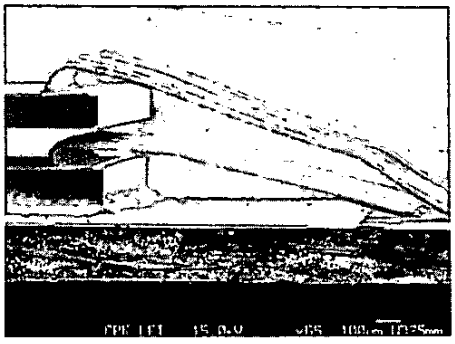

Figure 11. Cross-section of stacked die, where two integrated circuits have been stacked and wire-bonded to a package [26].

5. Conclusion

RFIC packaging technology is advancing very rapidly in an effort to keep pace with continuing developments in the IC technology area and emerging RF system applications. The standard wire bond connection to a lead frame plastic package remains the dominant technology, and improvements in package design and modelling will allow this technology to continue for many years. There are some new technologies on the horizon, which promise further improvements in performance — especially flip-chip and LTCC — but their increased cost may not justify the performance advantages except in niche applications. "Stacked" die approaches are a particularly attractive option in the future, where multiple die, each optimized for a particular application, reside in a common package.

6. Acknowledgment

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